EE 330
Lecture 31

Basic amplifier architectures

- Common Emitter/Source
- Common Collector/Drain
- Common Base/Gate

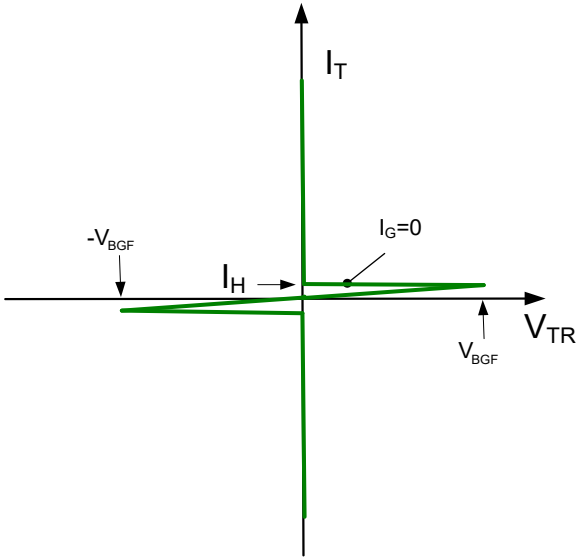
Spring 2024 Exam Schedule

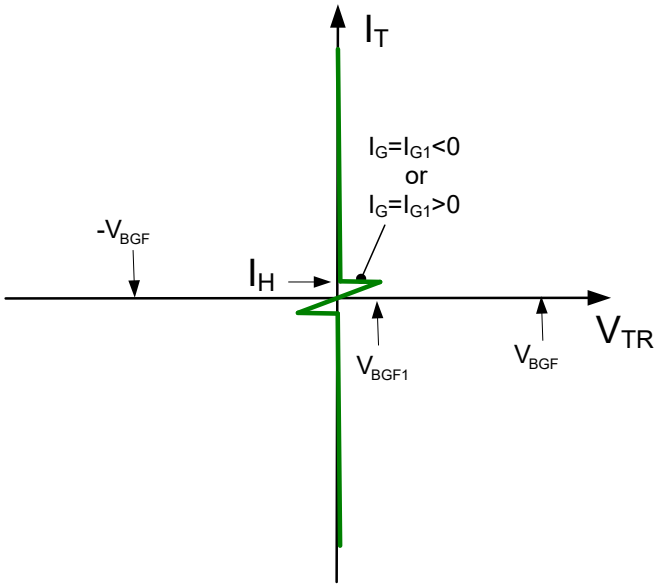
Exam 1	Friday Feb 16
Exam 2	Friday March 8
Exam 3	Friday April 19
Final Exam	Tuesday May 7 7:30 AM - 9:30 AM

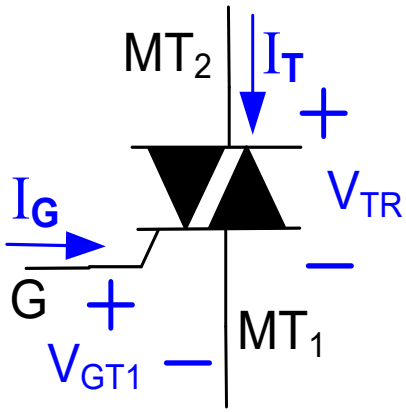
Review from Last Lecture

The Triac

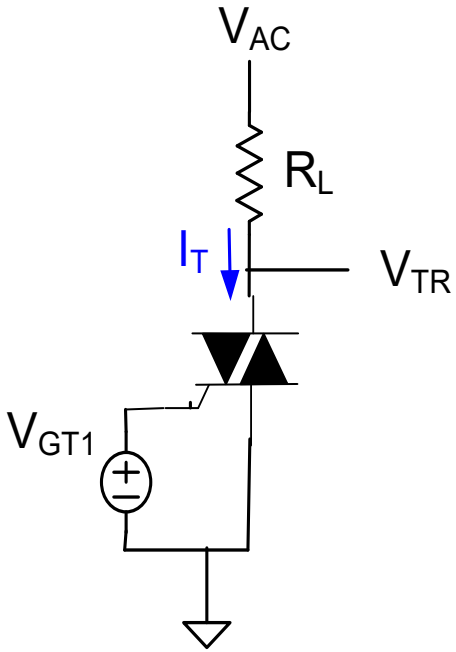
The ideal Triac





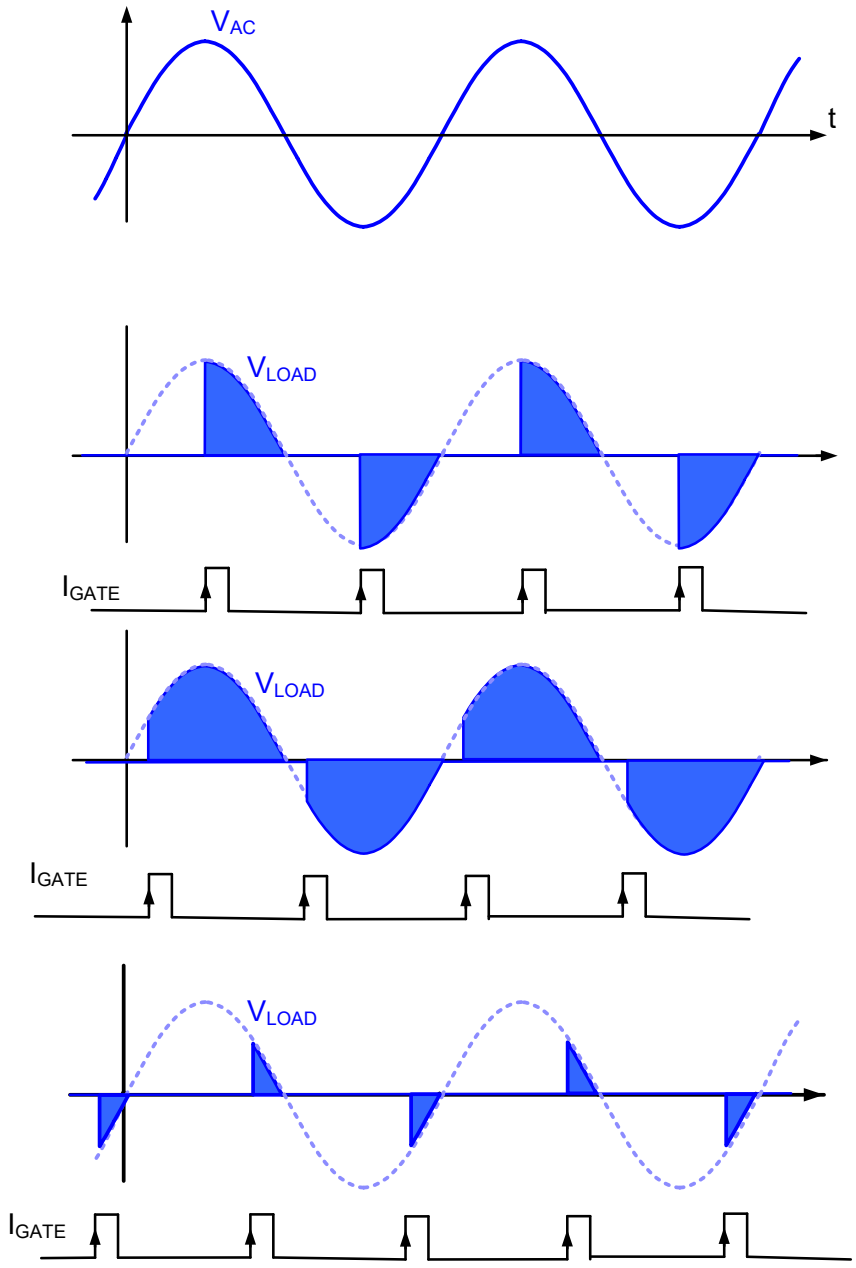


Consider the basic Triac circuit

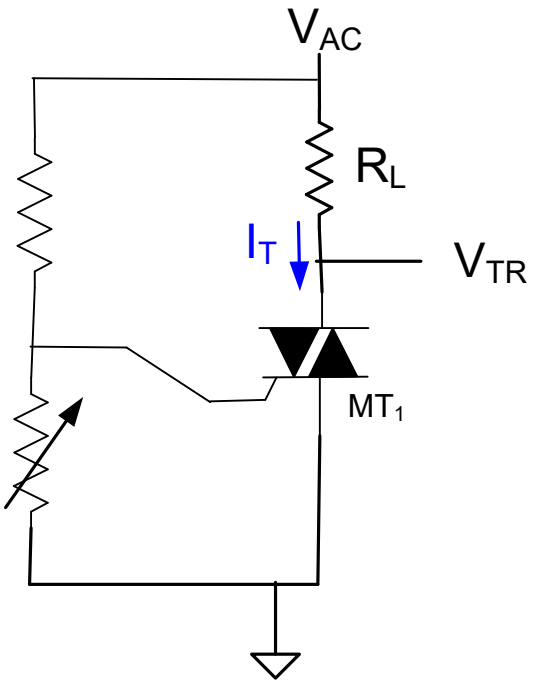


Review from Last Lecture

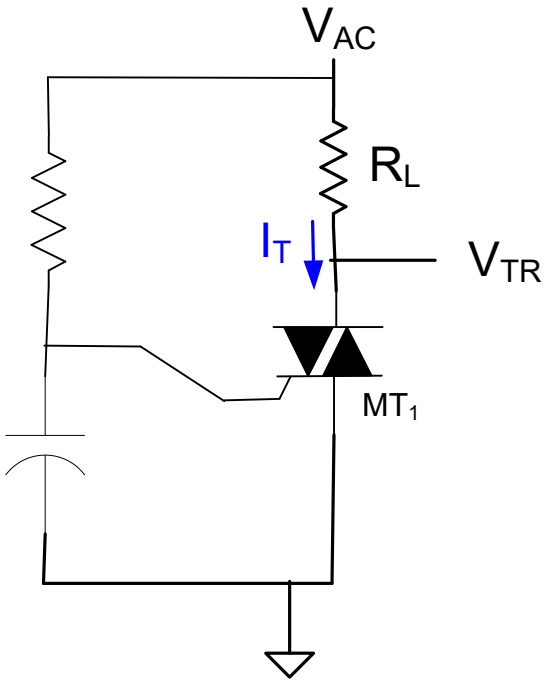
Phase controlled bidirectional switching with Triacs



Some Basic Triac Application Circuits

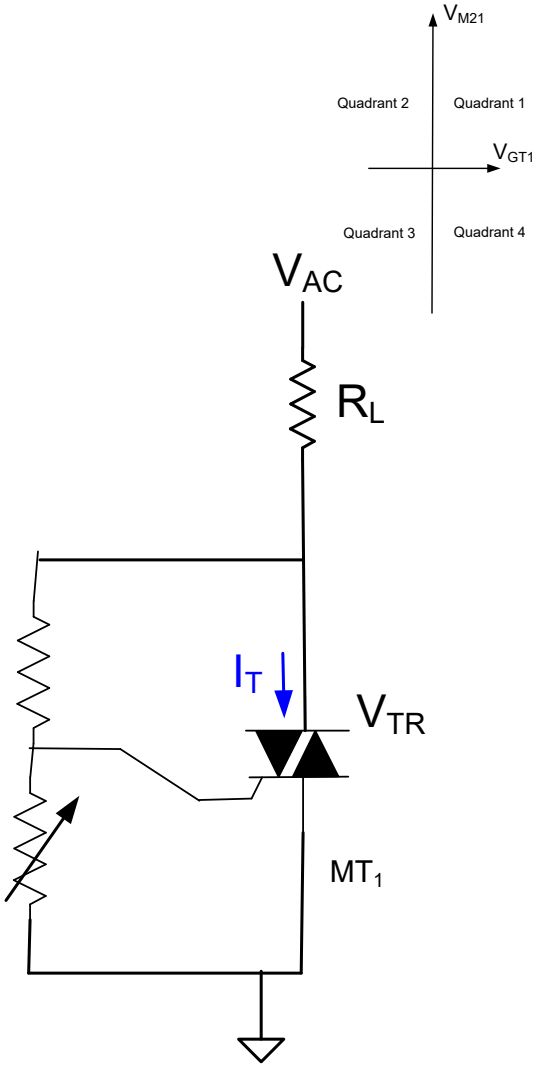


Quad 1 : Quad 3



Delays V_G signal to provide reduction in duty cycle

Quad 1 : Quad 3



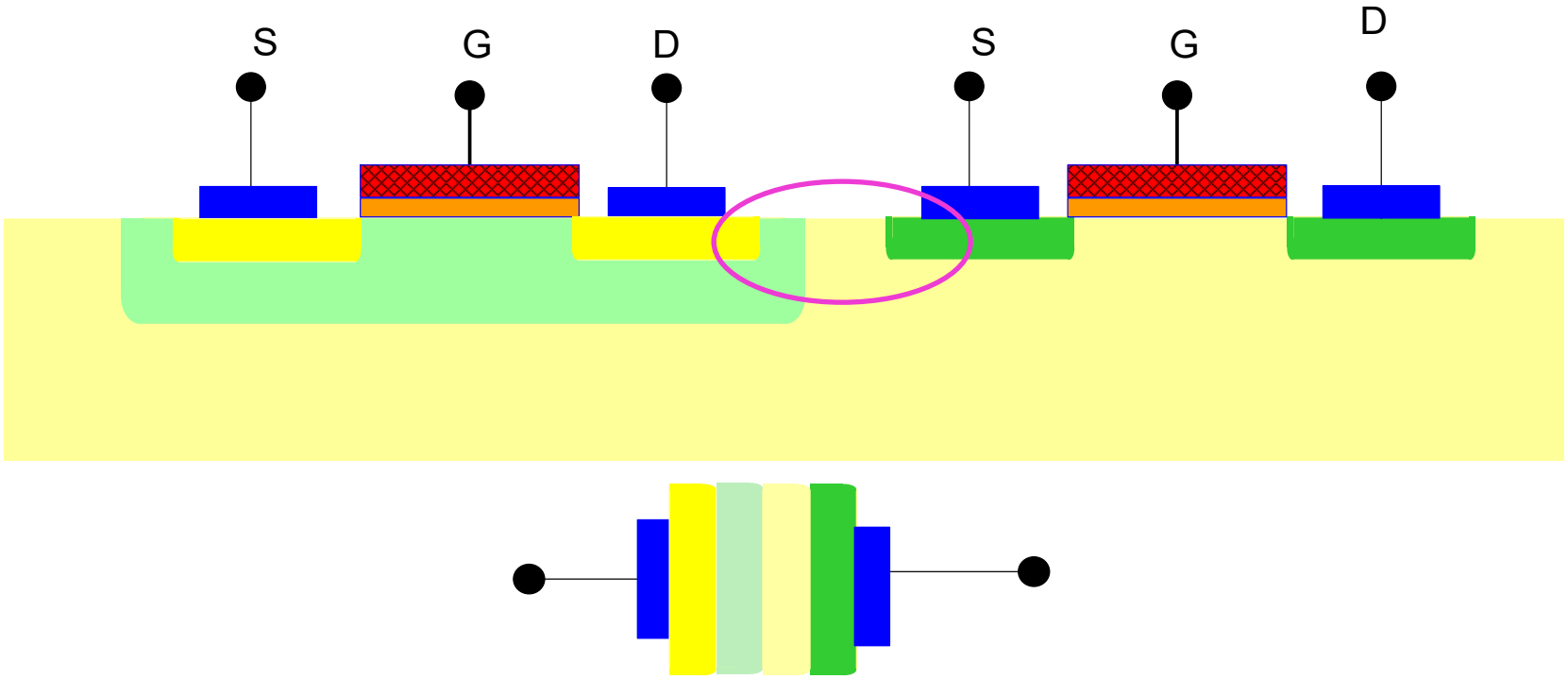
Quad 1 : Quad 3

Review from Last Lecture

The Thyristor

A bipolar device in CMOS Processes

Consider a Bulk-CMOS Process



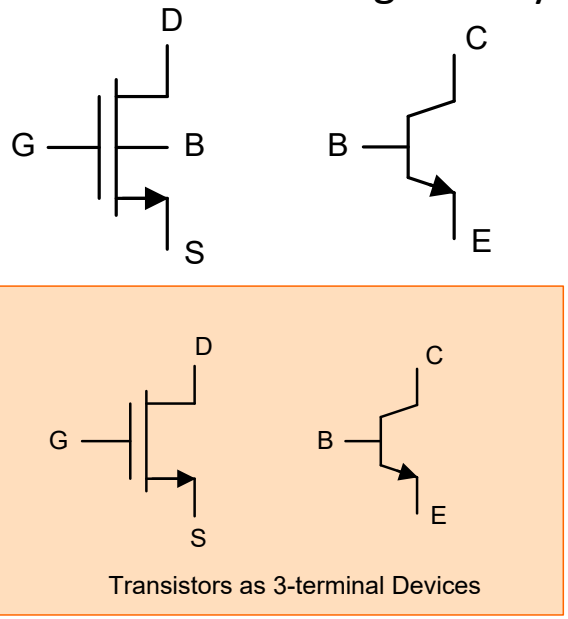
If this parasitic SCR turns on, either circuit will latch up or destroy itself

Guard rings must be included to prevent latchup

Design rules generally include provisions for guard rings

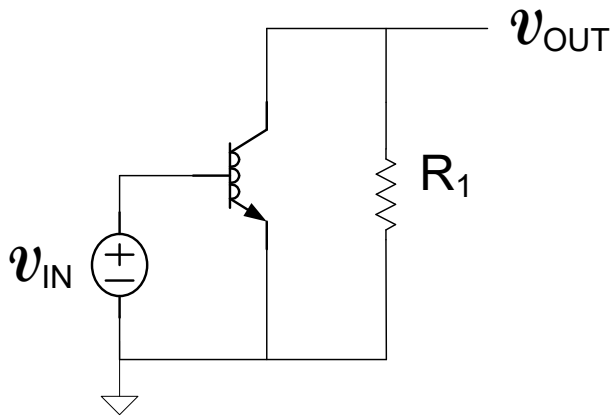
Basic Amplifier Structures

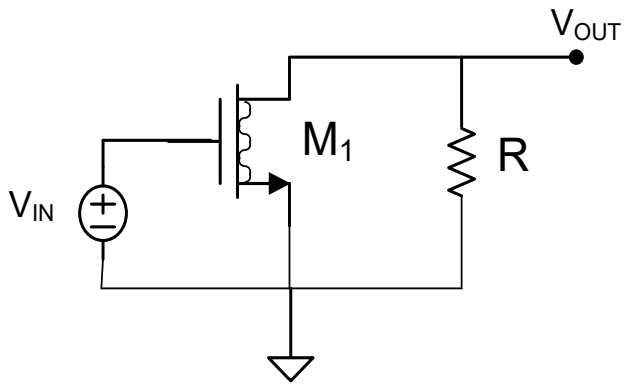
- MOS and Bipolar Transistors both have 3 primary terminals
- MOS transistor has a fourth terminal that is generally considered a parasitic terminal



Basic Amplifier Structures

Observation:



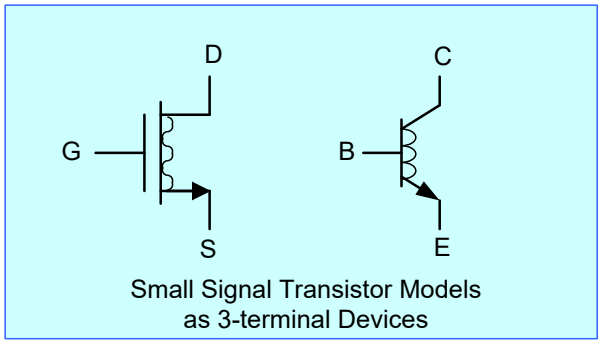


These circuits considered previously have a terminal (emitter or source) common to the input and output ports in the small-signal equivalent circuit

For BJT, E is common, input on B, output on C Termed "Common Emitter"

For MOSFET, S is common, input on G, output on D Termed "Common Source"

Basic Amplifier Structures



Small Signal Transistor Models
as 3-terminal Devices

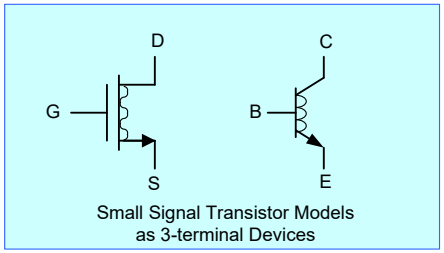
Amplifiers using these devices generally have one terminal common and use remaining terminals as input and output

Since devices are nearly unilateral, designation of input and output terminals is uniquely determined

Three different ways to designate the common terminal

Source or Emitter	termed Common Source or Common Emitter
Gate or Base	termed Common Gate or Common Base
Drain or Collector	termed Common Drain or Common Collector

Basic Amplifier Structures



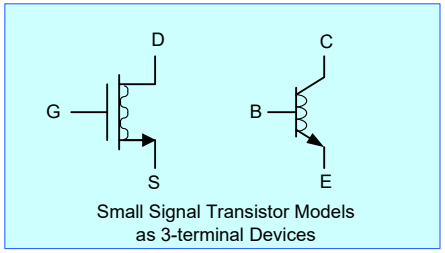
Small Signal Transistor Models
as 3-terminal Devices

	MOS			BJT		
	Common	Input	Output	Common	Input	Output
Common Source or Common Emitter	S	G	D	E	B	C
Common Gate or Common Base	G	S	D	B	E	C
Common Drain or Common Collector	D	G	S	C	B	E

Identification of Input and Output Terminals is not arbitrary

It will be shown that all 3 of the basic amplifiers are useful !

Basic Amplifier Structures



Small Signal Transistor Models
as 3-terminal Devices

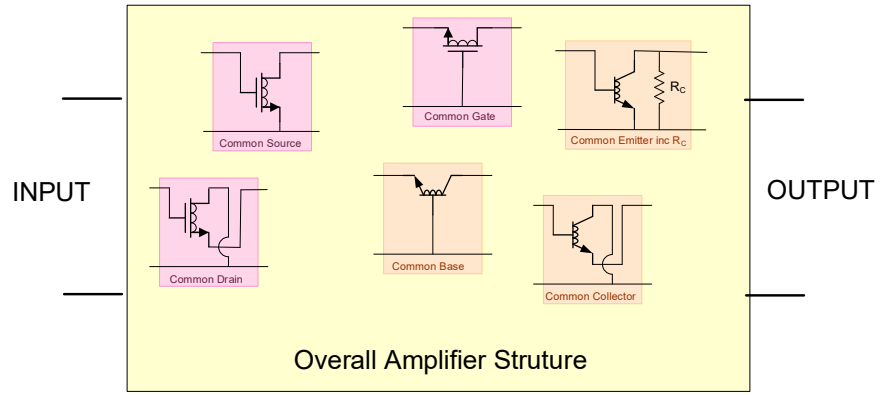
Common Source or Common Emitter

Common Gate or Common Base

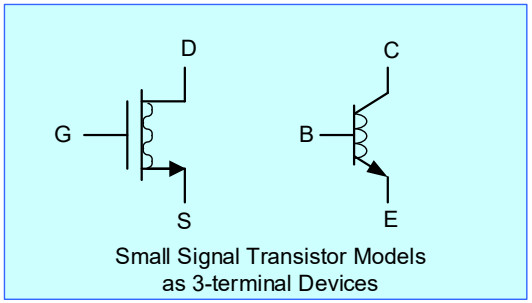
Common Drain or Common Collector

Objectives in Study of Basic Amplifier Structures

1. Obtain key properties of each basic amplifier
2. Develop method of designing amplifiers with specific characteristics using basic amplifier structures

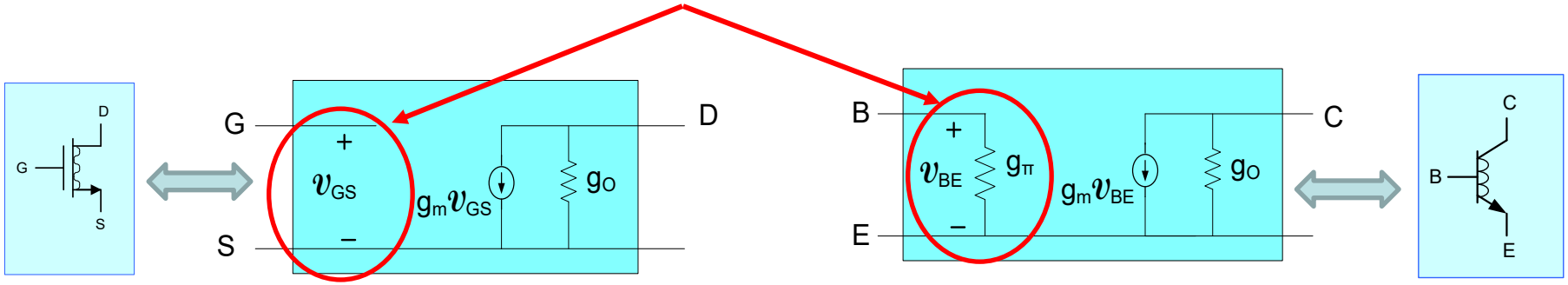


Characterization of Basic Amplifier Structures

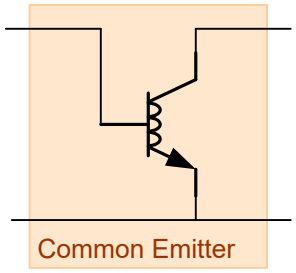


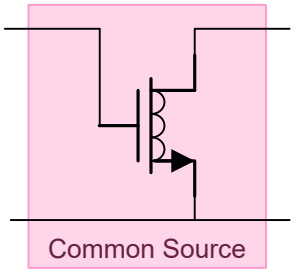
Small Signal Transistor Models
as 3-terminal Devices

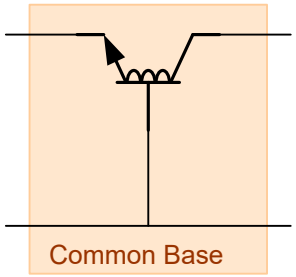
- Observe that the small-signal equivalent of any 3-terminal network is a two-port
- Thus to characterize any of the 3 basic amplifier structures, it suffices to determine the two-port equivalent network
- Since small signal model when expressed in terms of small-signal parameters of BJT and MOSFET differ only in the presence/absence of g_π term, can analyze the BJT structures and then obtain characteristics of corresponding MOS structure by setting $g_\pi=0$

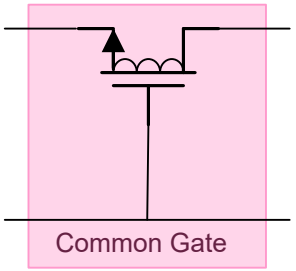


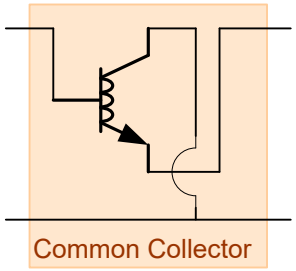
The three basic amplifier types for both MOS and bipolar processes

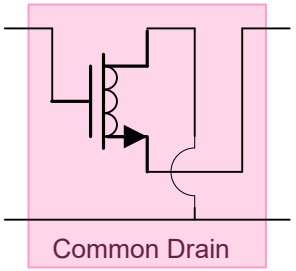






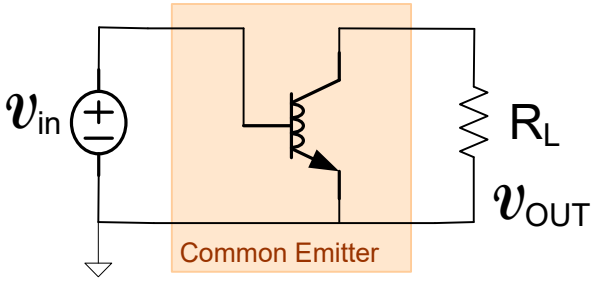


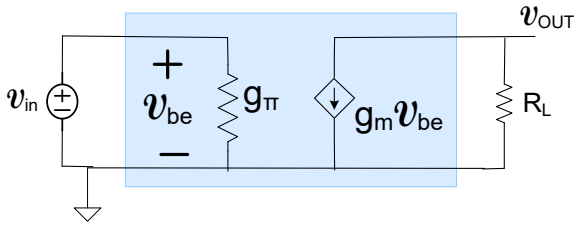




Will focus on the performance of the bipolar structures and then obtain performance of the MOS structures by observation

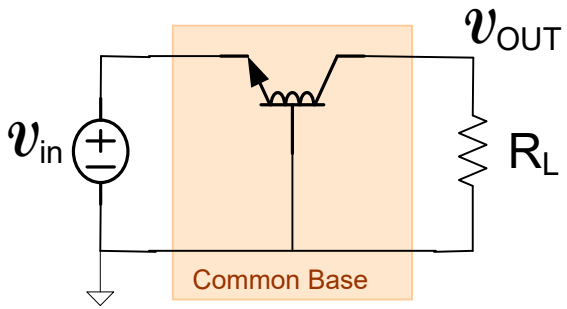
The three basic amplifier types for both MOS and bipolar processes

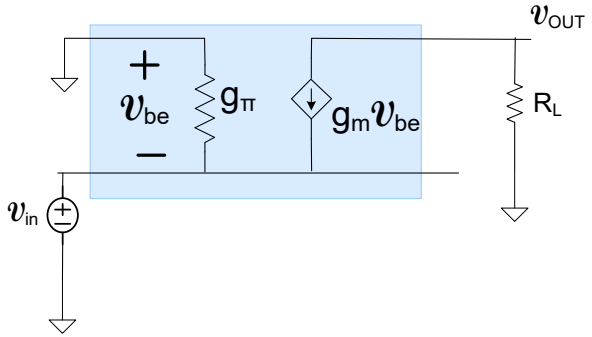




$$\left.\begin{aligned} v_{OUT} &= -g_m R_L v_{be} \\ v_{IN} &= v_{be} \end{aligned}\right\}$$

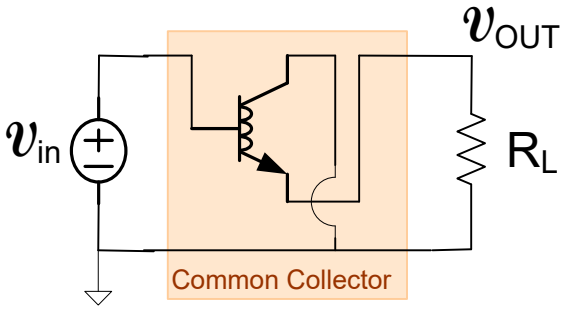
$$A_V = \frac{v_{OUT}}{v_{IN}} = -g_m R_L$$

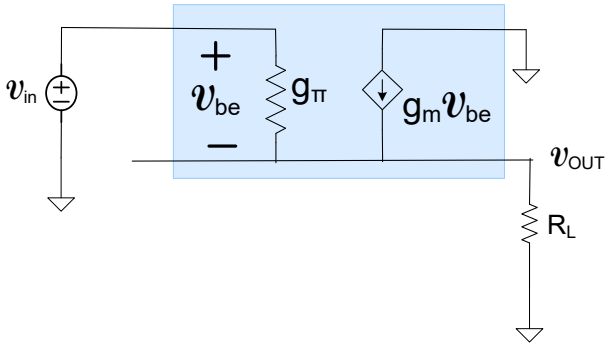




$$\left.\begin{aligned} v_{OUT} &= -g_m R_L v_{be} \\ v_{IN} &= -v_{be} \end{aligned}\right\}$$

$$A_V = \frac{v_{OUT}}{v_{IN}} = g_m R_L$$



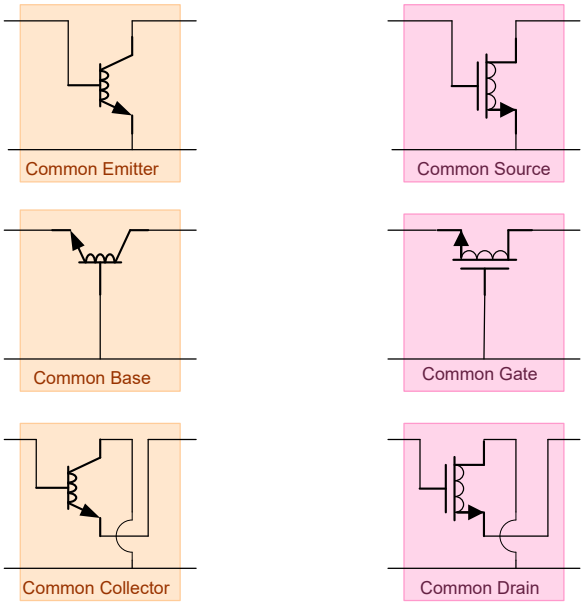


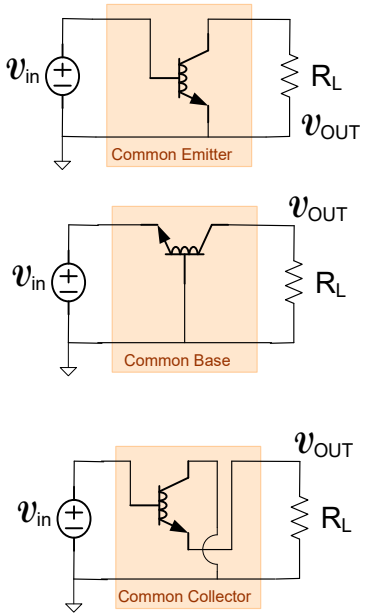
$$\left.\begin{aligned} v_{OUT} &= (g_m + g_\pi) v_{be} R_L \\ v_{IN} &= v_{be} + (g_m + g_\pi) v_{be} R_L \end{aligned}\right\}$$

$$A_V = \frac{v_{OUT}}{v_{IN}} = \frac{(g_m + g_\pi) R_L}{1 + (g_m + g_\pi) R_L} \cong 1$$

- Significantly different gain characteristics for the three basic amplifiers
- There are other significant differences too (R_{IN}, R_{OUT}, …) as well

The three basic amplifier types for both MOS and bipolar processes





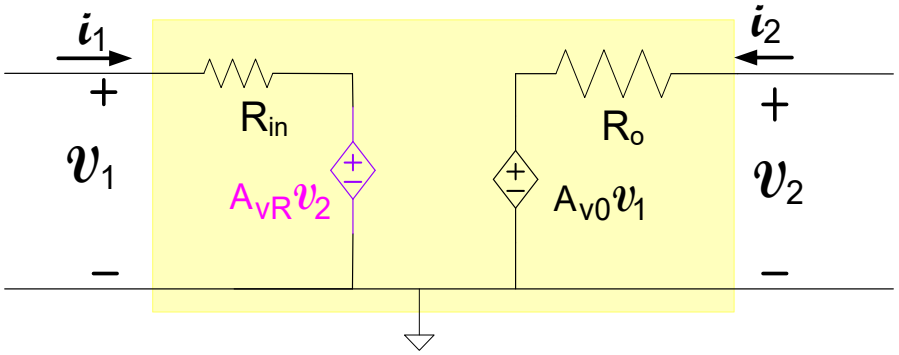
More general models are needed to accommodate biasing, understand performance capabilities, and include effects of loading of the basic structures

Two-port models are useful for characterizing the basic amplifier structures

How can the two-port parameters be obtained for these or any other linear two-port networks?

Two-Port Models of Basic Amplifiers widely used for Analysis and Design of Amplifier Circuits

Methods of Obtaining Amplifier Two-Port Network



1. v_{TEST} : i_{TEST} Method (considered in a previous lecture)

2. Write $v_1 : v_2$ equations in standard form

$$v_1 = i_1 R_{IN} + A_{VR} v_2$$
$$v_2 = i_2 R_O + A_{V0} v_1$$

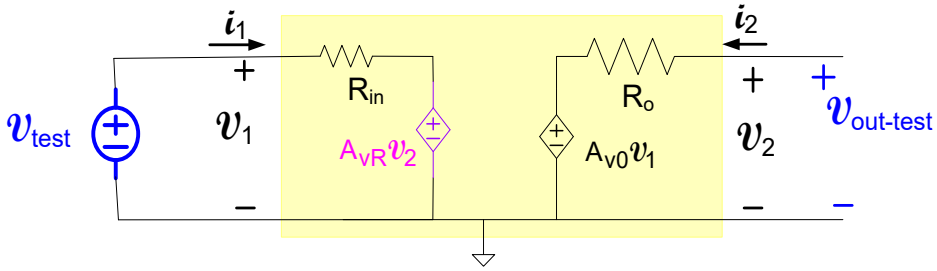
3. Thevenin-Norton Transformations

4. Ad Hoc Approaches

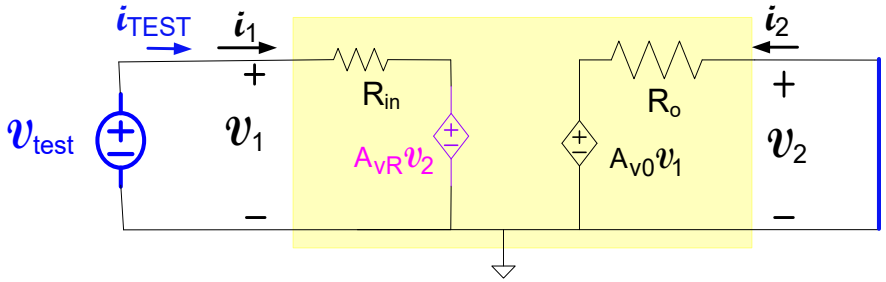
Any of these methods can be used to obtain the two-port model

$v_{test} : i_{test}$ Method for Obtaining Two-Port Amplifier Parameters

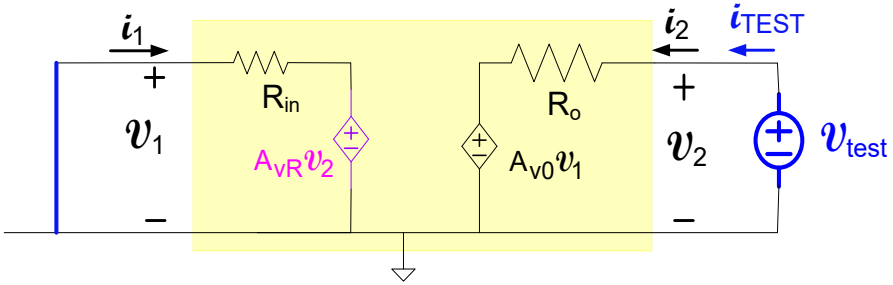
SUMMARY from PREVIOUS LECTURE



$$A_{V0} = \frac{v_{out\text{-}test}}{v_{test}}$$

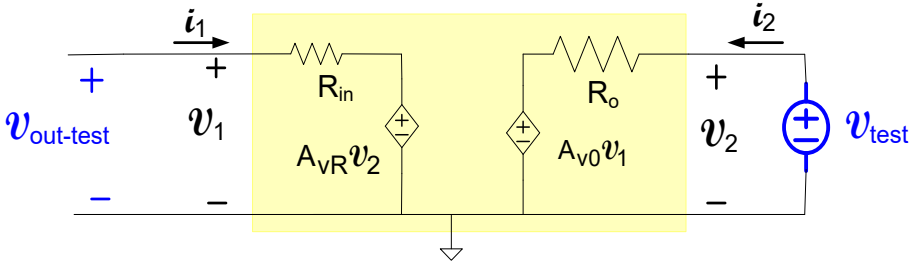


$$R_{in} = \frac{v_{test}}{i_{test}}$$



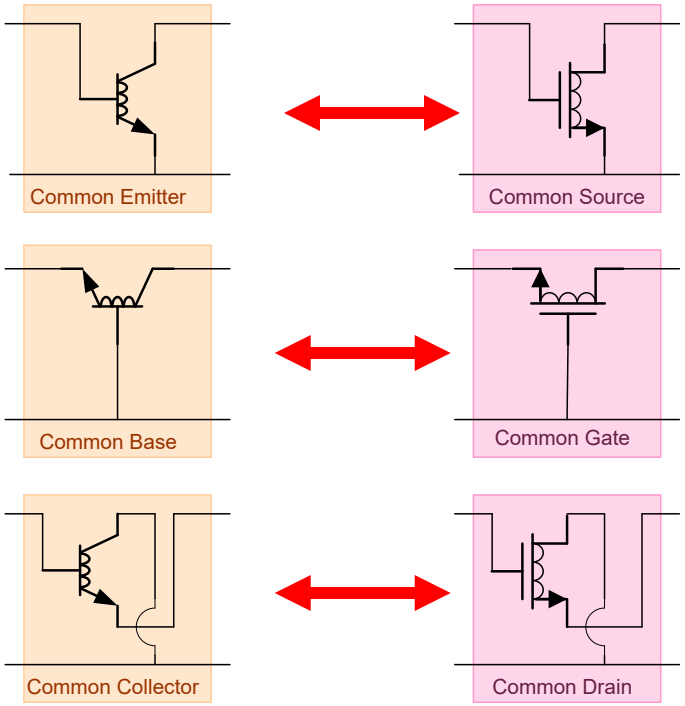
$$R_0 = \frac{v_{test}}{i_{test}}$$

If Unilateral $A_{VR} = 0$

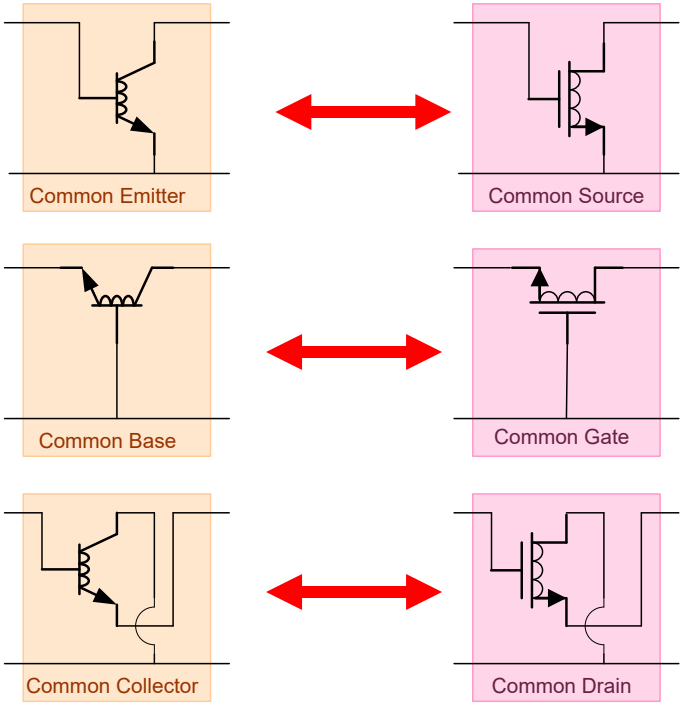


$$A_{VR} = \frac{v_{out\text{-}test}}{v_{test}}$$

Will now develop two-port model for each of the three basic amplifiers and look at one widely used application of each



Parameter Domains for Small-Signal Models for Any Devices



- Small-signal parameter domain

  Y-parameters, g-parameters, amplifier parameters, …

- Model Parameters and Operating Point (MPOP)

– Small-signal analysis naturally results in small-signal parameter domain
– More insight often in MPOP domain
– Mixed-parameter domains possible but often difficult to obtain insight

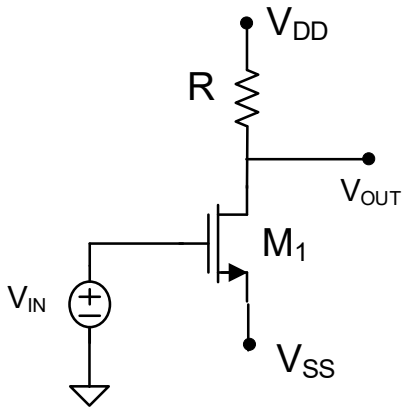
Parameter Domains for Small-Signal Models for Any Devices

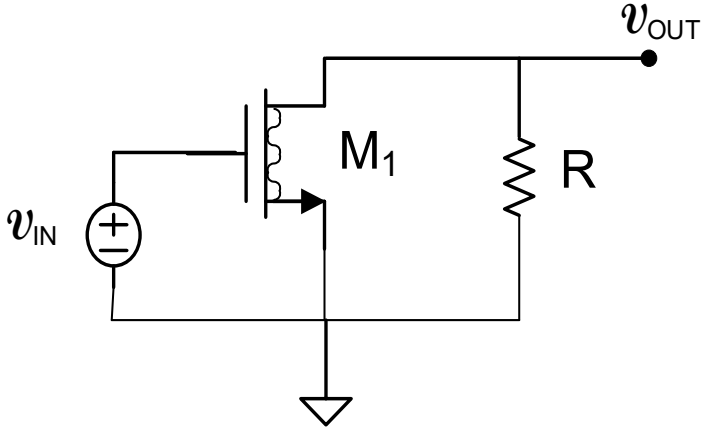
- Small-signal parameter domain

  Y-parameters, g-parameters, amplifier parameters, …

- Model Parameters and Operating Point (MPOP)

Example: Give A_V for basic amplifier in ss parameter domain and MPOP domain





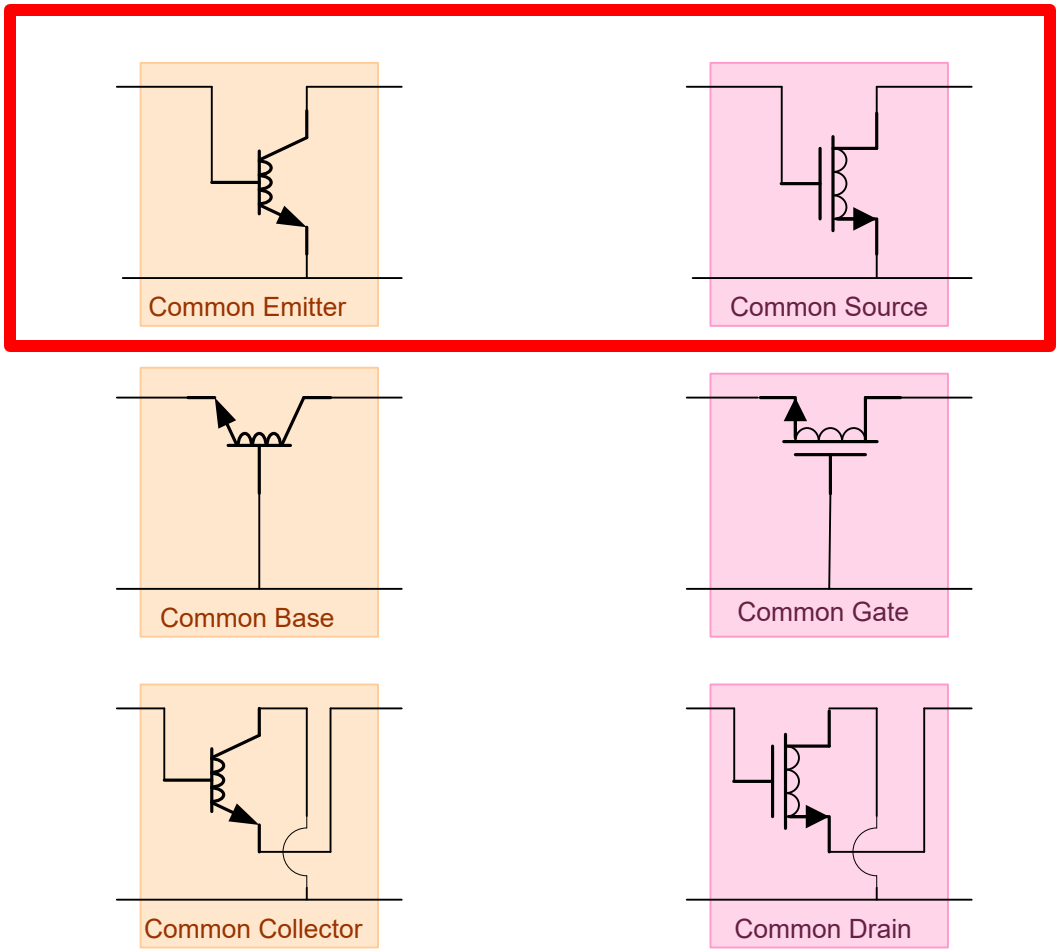
Small-Signal parameter domain

$$A_V = \frac{v_{OUT}}{v_{IN}} = -g_m R$$

MPOP domain

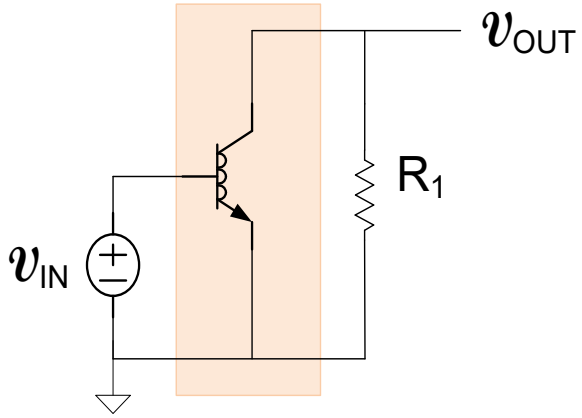
$$A_V = \frac{v_{OUT}}{v_{IN}} = -2\frac{I_{DQ}R}{V_{EB}}$$

Consider Common Emitter/Common Source Two-port Models

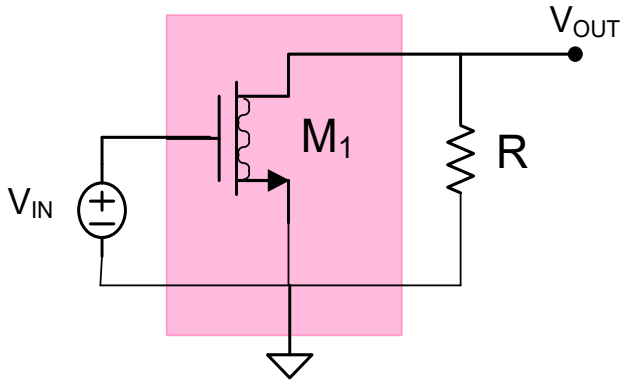


- Will focus on Bipolar Circuit since MOS counterpart is a special case obtained by setting $g_{\pi}=0$
- Will consider both two-port model and a widely used application

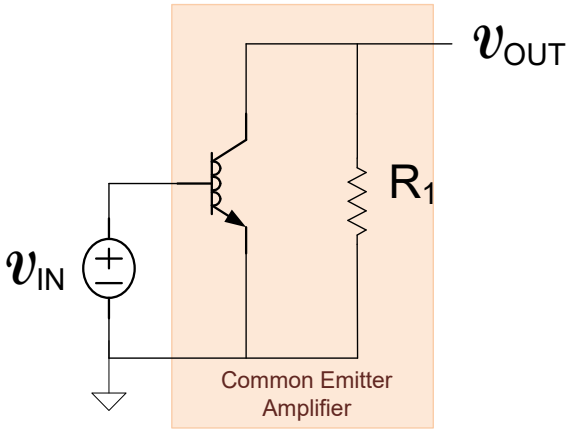
Basic CE/CS Amplifier Structures

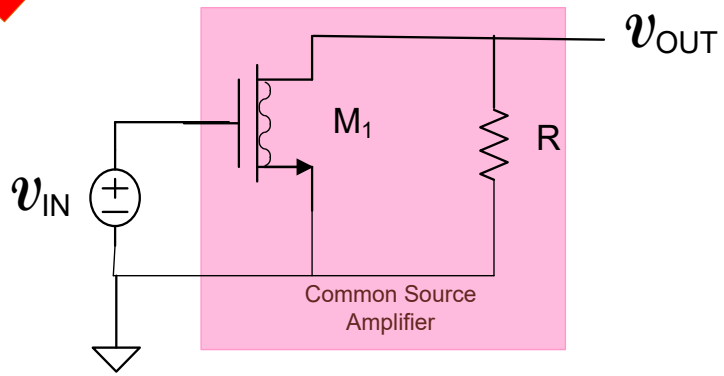


Common Emitter Amplifier



Common Source Amplifier

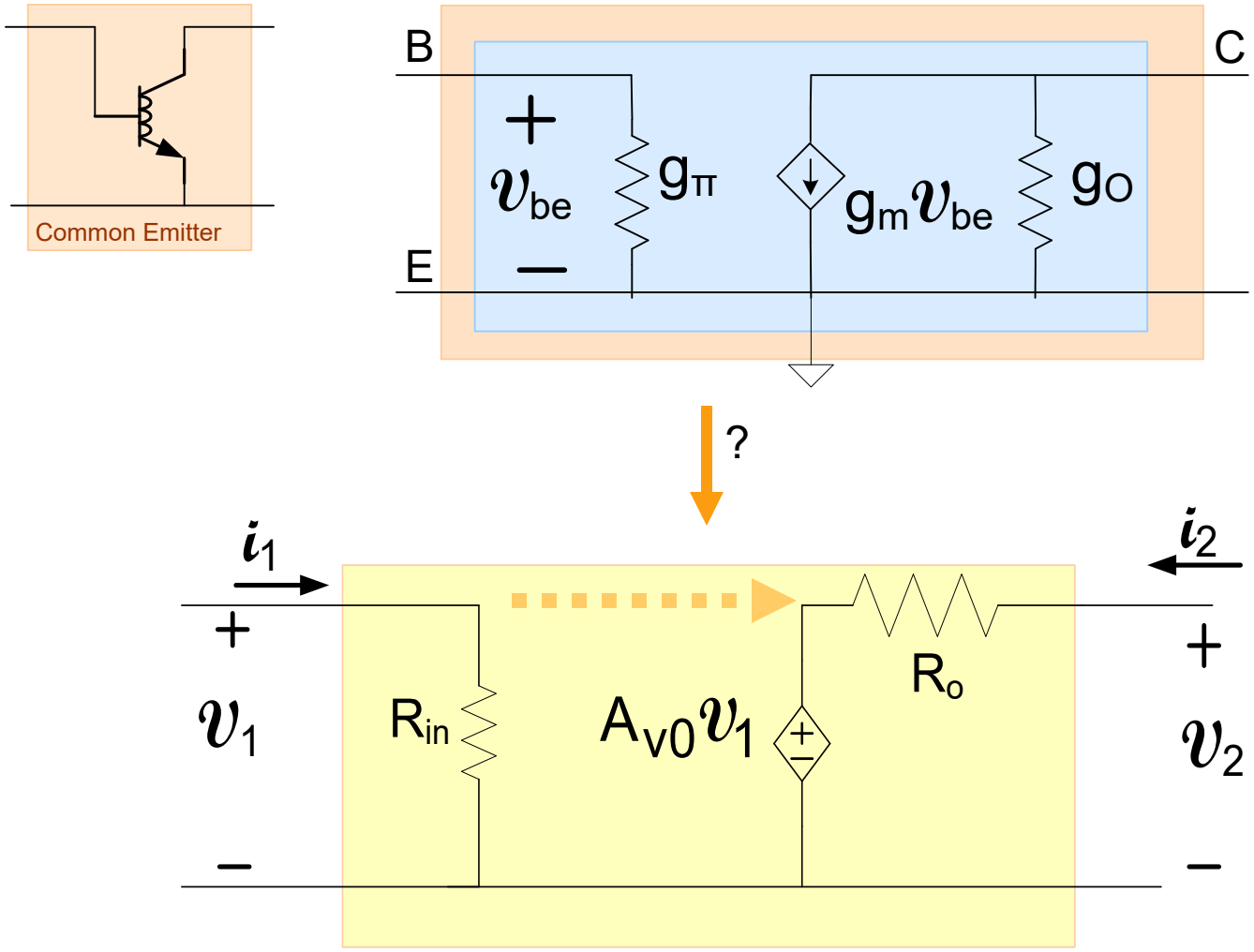




Can include or exclude R and R_1 in two-port models (of course they are different circuits)

The CE and CS amplifiers are themselves two-ports !

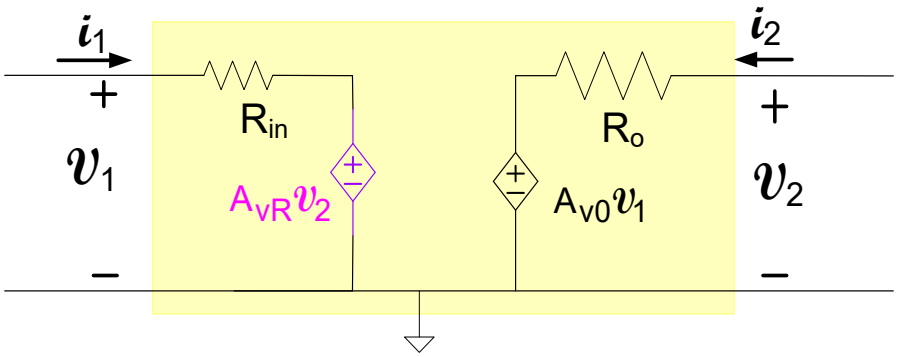
Two-port model for Common Emitter Configuration



{R_i, A_{V0} and R_0}

Two-Port Models of Basic Amplifiers widely used for Analysis and Design of Amplifier Circuits

Methods of Obtaining Amplifier Two-Port Network



1. v_{TEST} : i_{TEST} Method

2. Write $v_1 : v_2$ equations in standard form

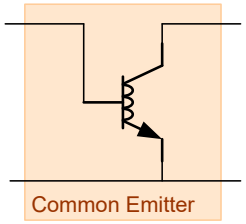
$$v_1 = i_1 R_{IN} + A_{VR} v_2$$

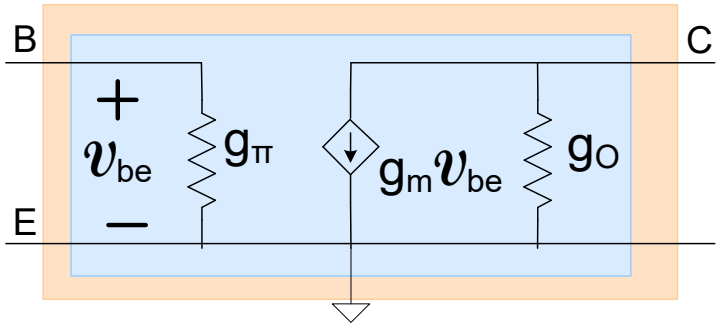
$$v_2 = i_2 R_O + A_{V0} v_1$$

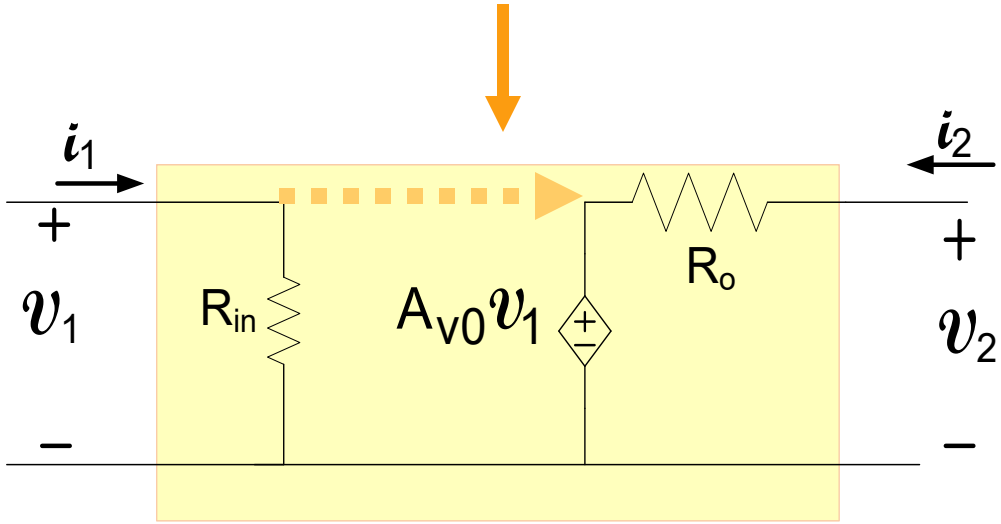
3. Thevenin-Norton Transformations

4. Ad Hoc Approaches

Two-port model for Common Emitter Configuration





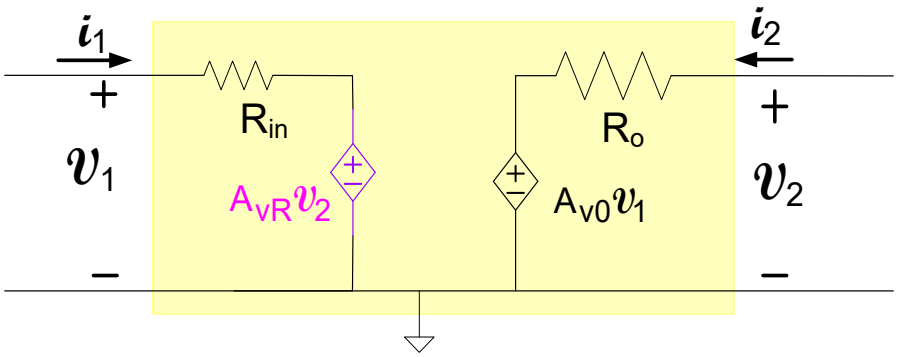


By Thevenin : Norton Transformations

$$R_{in} = \frac{1}{g_\pi} \qquad A_{V0} = -\frac{g_m}{g_0} \qquad R_0 = \frac{1}{g_0} \qquad A_{VR} = 0$$

Two-Port Models of Basic Amplifiers widely used for Analysis and Design of Amplifier Circuits

Methods of Obtaining Amplifier Two-Port Network



1. v_{TEST} : i_{TEST} method

2. Write $v_1 : v_2$ equations in standard form

$$v_1 = i_1 R_{IN} + A_{VR} v_2$$

$$v_2 = i_2 R_O + A_{V0} v_1$$

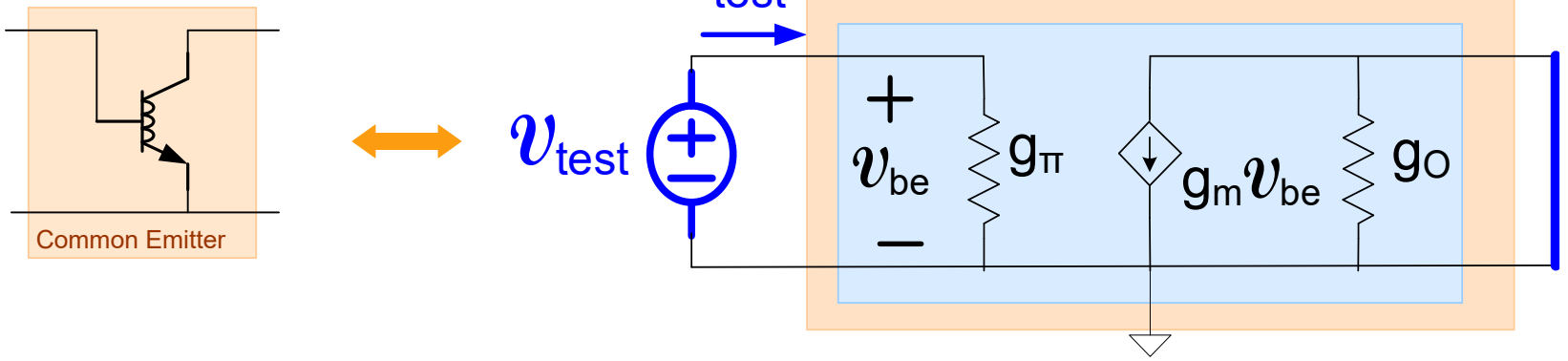
3. Thevenin-Norton Transformations

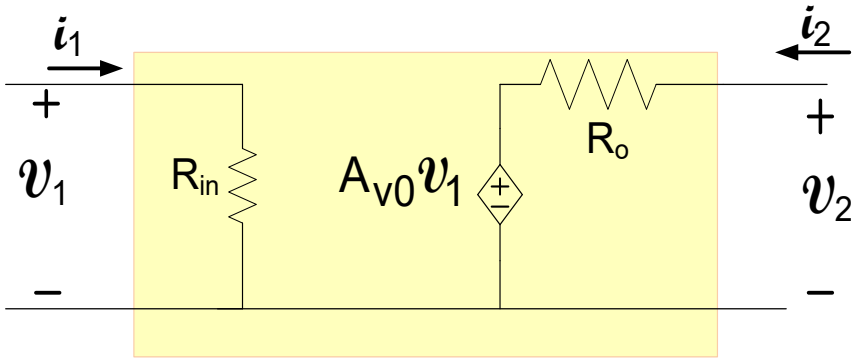
4. Ad Hoc Approaches

Two-port model for Common Emitter Configuration

Alternately, by v_{TEST} : i_{TEST} Method

To obtain R_{in}





$$R_{in} = \frac{v_{test}}{i_{test}}$$

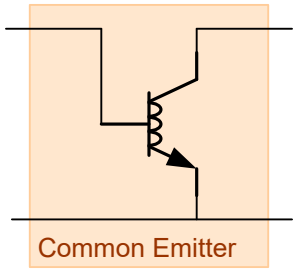
$$R_{in} = \frac{1}{g_{\pi}}$$

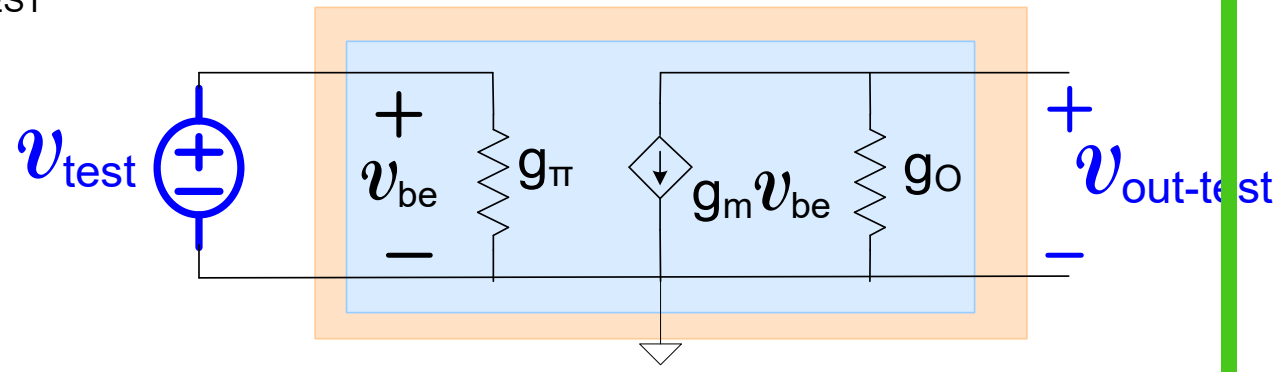
{R_{in}, A_{V0} and R_0}

Two-port model for Common Emitter Configuration

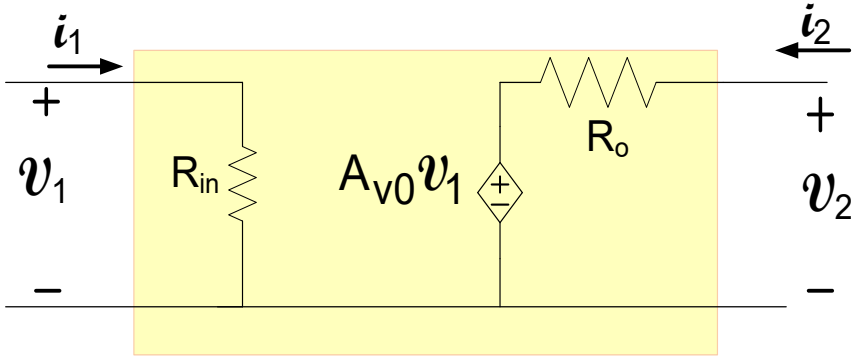
Alternately, by v_{TEST} : i_{TEST} Method

To obtain A_{V0}





$$A_{V0} = \frac{v_{out\text{-}test}}{v_{test}}$$



$$v_{out-test} = v_{test}\left(-\frac{g_m}{g_0}\right)$$

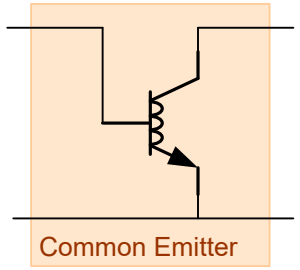
$$A_{V0} = -\frac{g_m}{g_0}$$

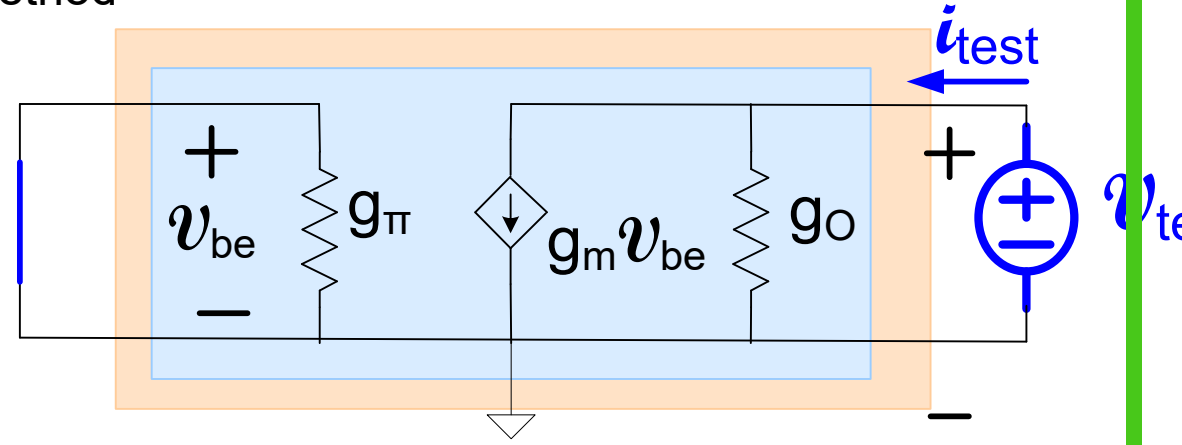
{R_{in}, A_{V0} and R_0}

Two-port model for Common Emitter Configuration

Alternately, by v_{TEST} : i_{TEST} Method

To obtain g_0

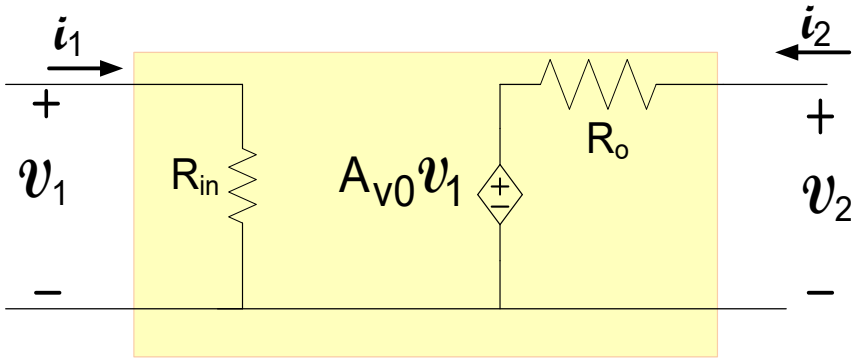




$$R_0 = \frac{v_{test}}{i_{test}}$$

$$v_{test} = i_{test}\,(g_0)$$

$$R_0 = \frac{1}{g_0}$$



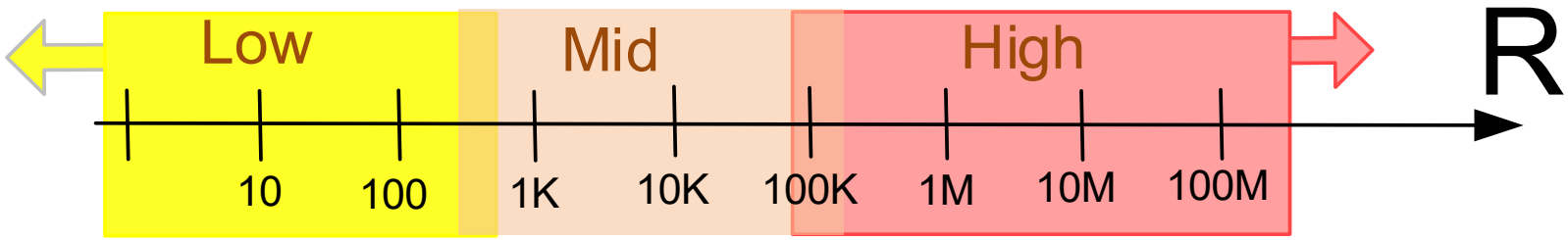
{R_{in}, A_{V0} and R_0}

Impedance Range and Classification

The terms “High Impedance” and “ Low Impedance” are often used

Whether an impedance is considered high or low or mid-range is a relative assessment

When building MOS or BJT amplifiers, the following relative notation of impedance levels is often useful (though there may be some extreme applications where even this notation is not standard)

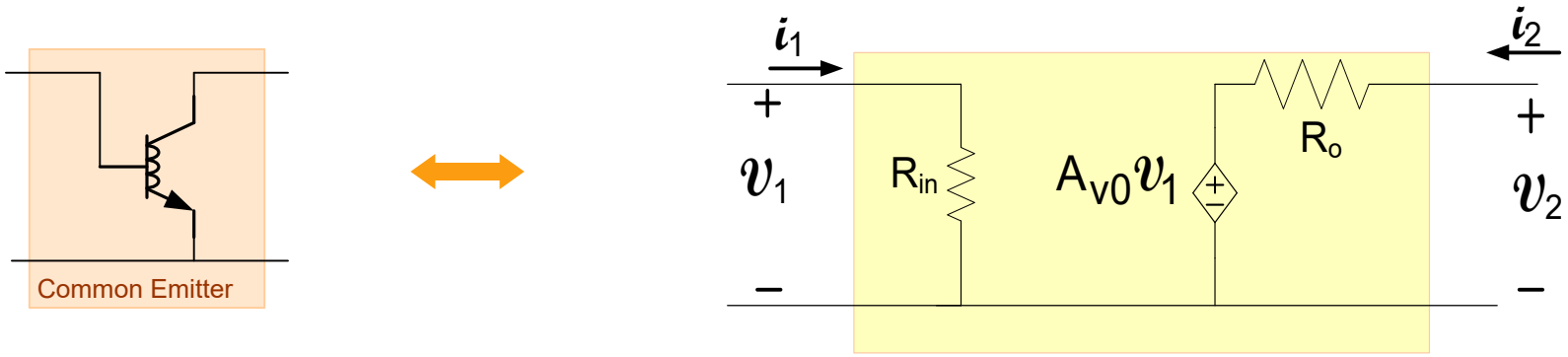


Impedance Range and Classification

Ideal Port Impedance of the four basic amplifiers

Amplifier Type	R_{IN}	R_{OUT}
Voltage	∞	0
Current	0	∞
Transconductance	∞	∞
Transresistance	0	0

Two-port model for Common Emitter Configuration



In terms of small signal model parameters:

$$R_{in} = \frac{1}{g_\pi} \qquad A_{V0} = -\frac{g_m}{g_0} \qquad R_0 = \frac{1}{g_0} \qquad A_{VR} = 0$$

In terms of operating point and model parameters:

$$R_i = \frac{\beta V_t}{I_{CQ}} \qquad A_{V0} = -\frac{V_{AF}}{V_t} \qquad R_0 = \frac{V_{AF}}{I_{CQ}} \qquad A_{VR} = 0$$

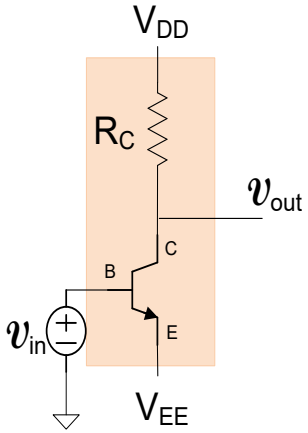
Characteristics:

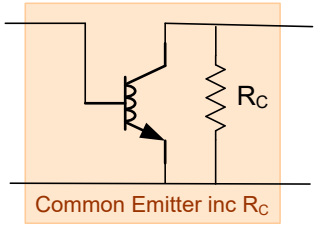
- Input impedance is mid-range
- Voltage Gain is Large and Inverting
- Output impedance is large
- Unilateral
- Widely used to build voltage amplifiers

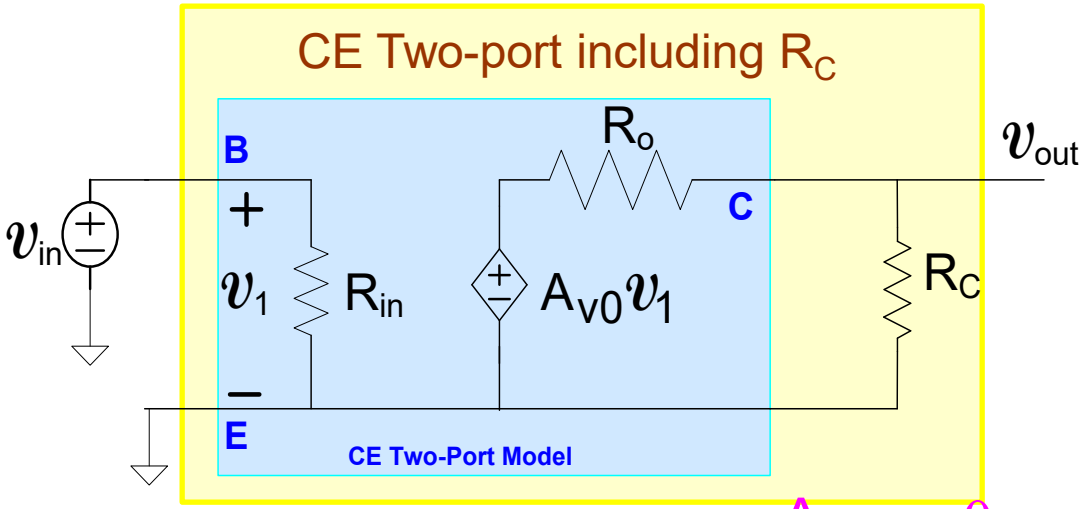
Common Emitter Configuration

Consider the following CE application

(this will also generate a two-port model for this CE application)







$$g_C \underset{def}{=} \frac{1}{R_C}$$

$$\frac{g_o}{g_C} = \frac{I_{CQ}R_C}{V_{AF}} << 1$$

$A_{VR} = 0$

$$v_{out}\left(g_C + g_0\right) = g_0 A_{V0} v_{in} \rightarrow A_{VC} = \frac{v_{out}}{v_{in}} = \frac{g_0 A_{V0}}{g_0 + g_C} = \frac{-g_m}{g_0 + g_C} \overset{g_0 << g_C}{\cong} -g_m R_C$$

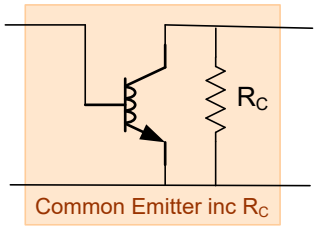
$$R_{inC} = R_{in} = r_\pi$$

$$R_{outC} = R_o // R_C \rightarrow R_{outC} = R_o // R_C = \frac{1}{g_0 + g_C} \overset{g_0 << g_C}{\cong} R_C$$

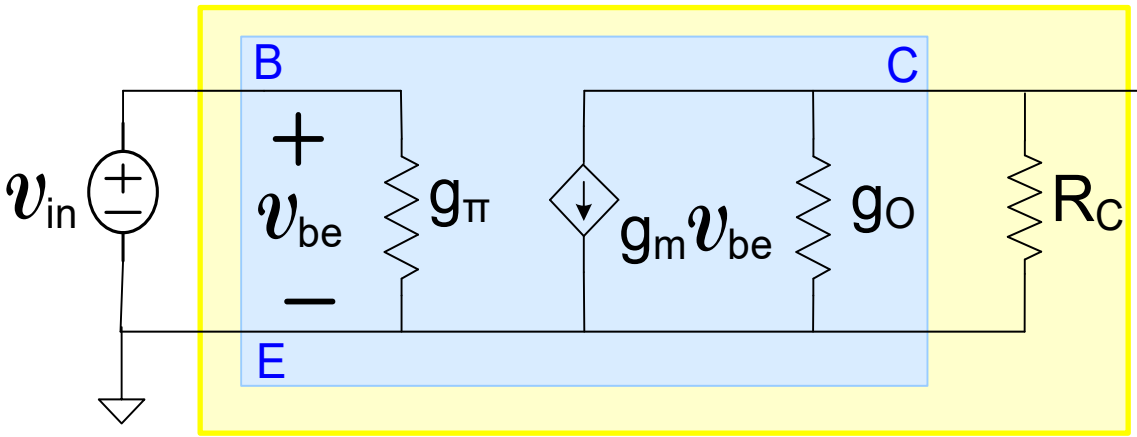
Common Emitter Configuration

Consider the following CE application

(this will also generate a two-port model for this CE application)



This circuit can also be analyzed directly without using 2-port model for CE configuration (use standard 2-port transistor model instead)



$$g_C \underset{def}{=} \frac{1}{R_C}$$

$$\frac{g_O}{g_C} = \frac{I_{CQ}R_C}{V_{AF}} << 1$$

$$A_{VR} = 0$$

$$v_{out} = -g_m v_{in}\left(\frac{1}{g_0 + g_C}\right) \rightarrow A_v = \frac{v_{out}}{v_{in}} = -\left(\frac{g_m}{g_0 + g_C}\right) \overset{g_0 << g_C}{\cong} -g_m R_C$$

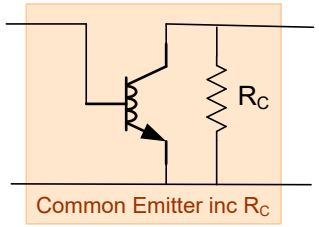
$$R_{in} = r_\pi$$

$$R_{out} = \frac{1}{g_0 + g_C} \overset{g_0 << g_C}{\cong} R_C$$

Common Emitter Configuration

Consider the following CE application

(this is also a two-port model for this CE application)



Small-signal parameter domain

$$A_v \overset{g_0 << g_C}{\cong} -g_m R_C$$

$$R_{out} = \frac{1}{g_0 + g_C} \overset{g_0 << g_C}{\cong} R_C$$

$$R_{in} = r_\pi$$

Operating point and model parameter domain

$$A_v \overset{g_0 << g_C}{\cong} -\frac{I_{CQ} R_C}{V_t}$$

$$R_{out} \overset{g_0 << g_C}{\cong} R_C$$

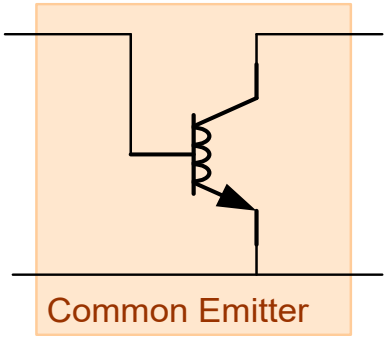
$$R_{in} = \frac{\beta V_t}{I_{CQ}}$$

$$A_{VR} = 0$$

Characteristics:

- Input impedance is mid-range
- Voltage Gain is large and Inverting
- Output impedance is mid-range
- Unilateral
- Widely used as a voltage amplifier

Common Source/ Common Emitter Configurations

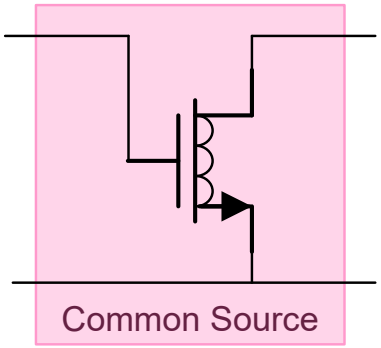


$A_{VR} = 0$

$$R_{in} = \frac{1}{g_\pi} \qquad A_{V0} = -\frac{g_m}{g_0} \qquad R_0 = \frac{1}{g_0}$$

$A_{VR} = 0$

$$R_{in} = \infty \qquad A_{V0} = -\frac{g_m}{g_0} \qquad R_0 = \frac{1}{g_0}$$



In terms of operating point and model parameters:

$$R_{in} = \frac{\beta V_t}{I_{CQ}} \qquad A_{V0} = -\frac{V_{AF}}{V_t} \qquad R_0 = \frac{V_{AF}}{I_{CQ}}$$

$$R_{in} = \infty \qquad R_0 = \frac{1}{\lambda I_{DQ}} = \frac{V_{AF}}{I_{DQ}}$$

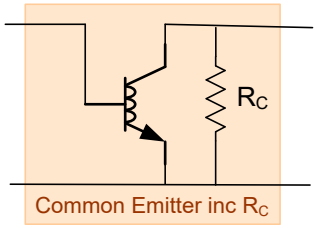
$$A_{V0} = -\frac{2}{\lambda V_{EBQ}} = -2\frac{V_{AF}}{V_{EBQ}}$$

Characteristics:

- Input impedance is mid-range (infinite for MOS)
- Voltage Gain is Large and Inverting
- Output impedance is large
- Unilateral
- Widely used to build voltage amplifiers

Common Source/Common Emitter Configuration

Widely used CE application (but also a two-port)

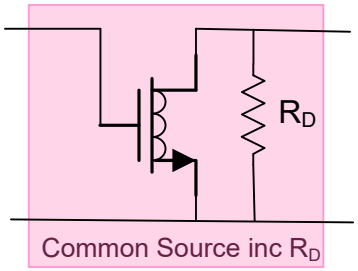


$$R_{out} = \frac{1}{g_0 + g_C} \overset{g_0 << g_C}{\cong} R_C$$

$$A_v \overset{g_0 << g_C}{\cong} -g_m R_C$$

$R_{in} = r_\pi$

$A_{VR} = 0$



$$R_{out} = \frac{1}{g_0 + g_D} \overset{g_0 << g_D}{\cong} R_D$$

$$A_v \overset{g_0 << g_D}{\cong} -g_m R_D$$

$A_{VR} = 0$

$R_{in} = \infty$

In terms of operating point and model parameters:

$$A_v \overset{g_0 << g_C}{\cong} -\frac{I_{CQ} R_C}{V_t}$$

$$R_{out} \overset{g_0 << g_C}{\cong} R_C$$

$$R_{in} = \frac{\beta V_t}{I_{CQ}}$$

$$A_v \overset{g_0 << g_D}{\cong} -\frac{2 I_{DQ} R_D}{V_{EBQ}}$$

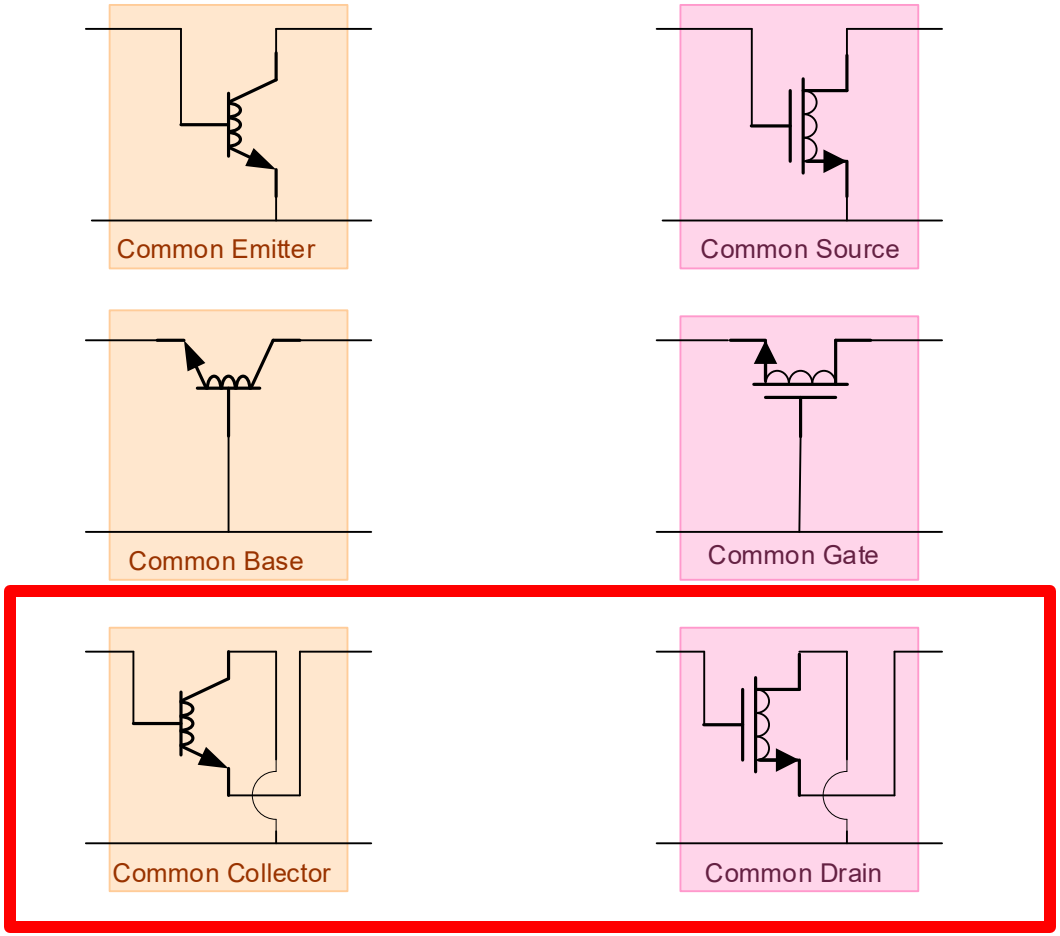
$R_{in} = \infty$

$$R_{out} \overset{g_0 << g_D}{\cong} R_D$$

Characteristics:

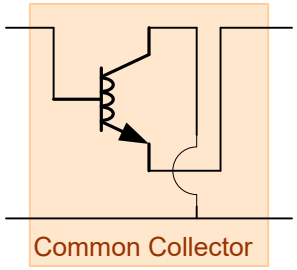
- Input impedance is mid-range (infinite for MOS)
- Voltage Gain is Large and Inverting
- Output impedance is mid-range
- Unilateral
- Widely used as a voltage amplifier

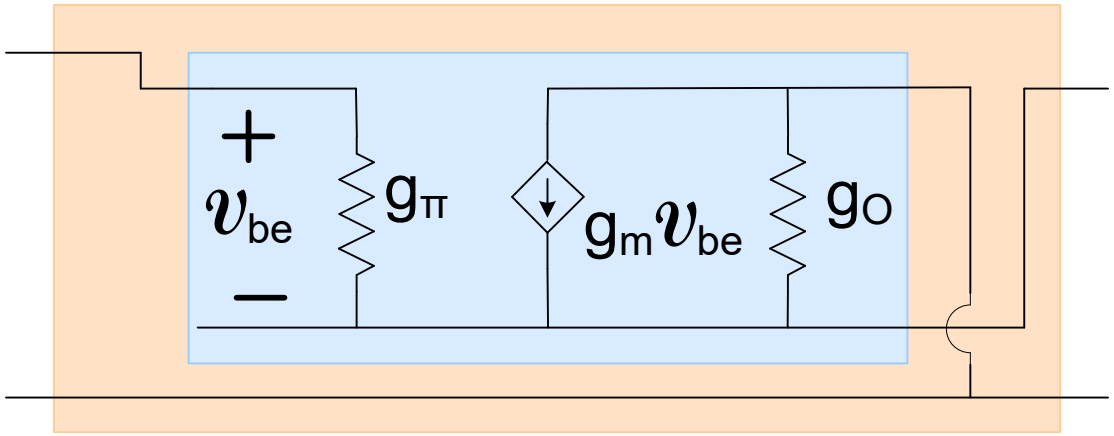
Consider Common Collector/Common Drain Two-port Models



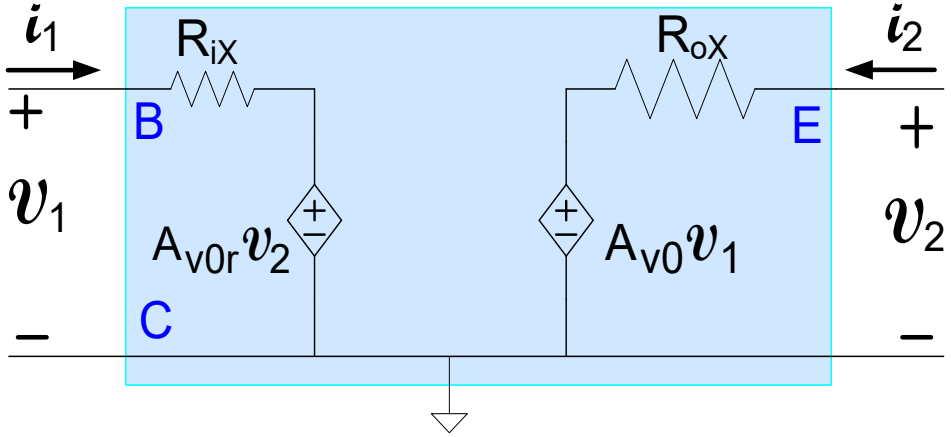
- Will focus on Bipolar Circuit since MOS counterpart is a special case obtained by setting $g_{\pi}=0$
- Will consider both two-port model and a widely used application

Two-port model for Common Collector Configuration





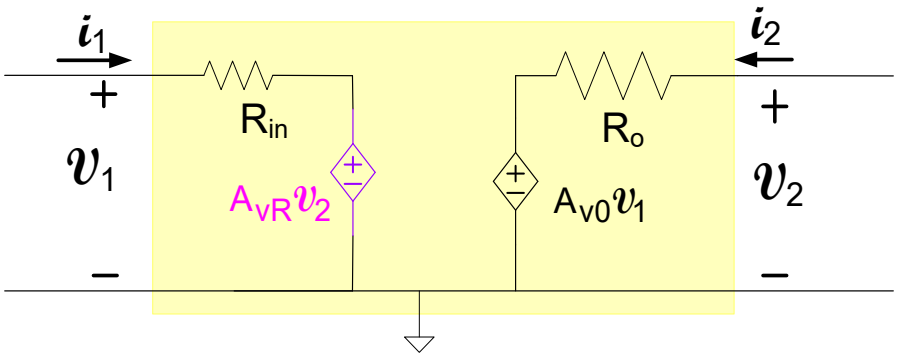
?



{R_{iX}, A_{V0}, A_{V0r} and R_{0X}}

Two-Port Models of Basic Amplifiers widely used for Analysis and Design of Amplifier Circuits

Methods of Obtaining Amplifier Two-Port Network



1. v_{TEST} : i_{TEST} Method

2. Write $v_1 : v_2$ equations in standard form

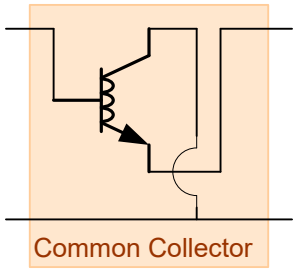
$$v_1 = i_1 R_{IN} + A_{VR} v_2$$

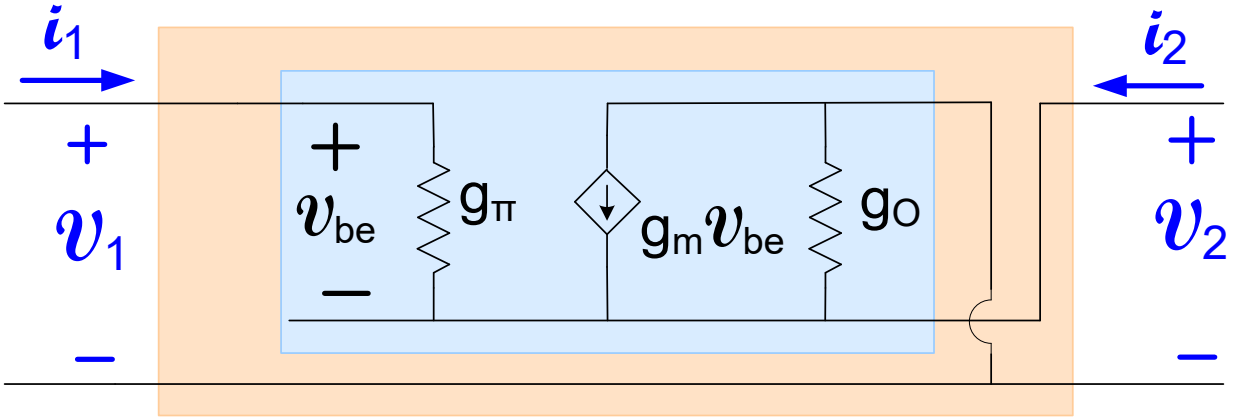
$$v_2 = i_2 R_O + A_{V0} v_1$$

3. Thevenin-Norton Transformations

4. Ad Hoc Approaches

Two-port model for Common Collector Configuration

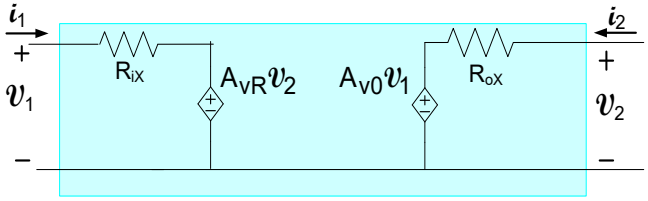




Applying KCL at the input and output node, obtain

$$i_1 = (v_1 - v_2)\,g_\pi$$
$$i_2 = (g_m + g_\pi + g_o)\,v_2 - (g_m + g_\pi)\,v_1$$

Standard Two-Port Amplifier Representation



$$v_1 = i_1 R_{iX} + A_{VR} v_2$$
$$v_2 = i_2 R_{oX} + A_V v_1$$

$v_1 : v_2$ equations in standard form

These can be rewritten as

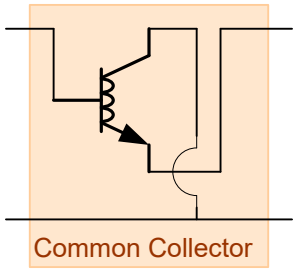
$$v_1 = i_1 r_\pi + v_2$$
$$v_2 = \left(\frac{1}{g_m + g_\pi + g_o}\right) i_2 + \left(\frac{g_m + g_\pi}{g_m + g_\pi + g_o}\right) v_1$$

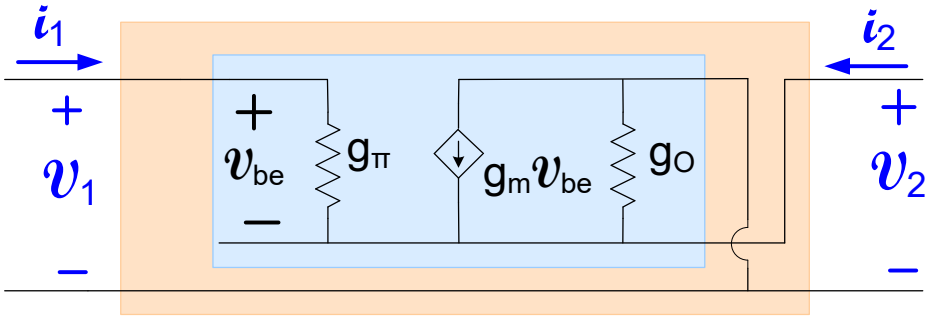
It thus follows that

$R_{iX} = r_\pi$ $\quad$ $A_{VOr} = 1$

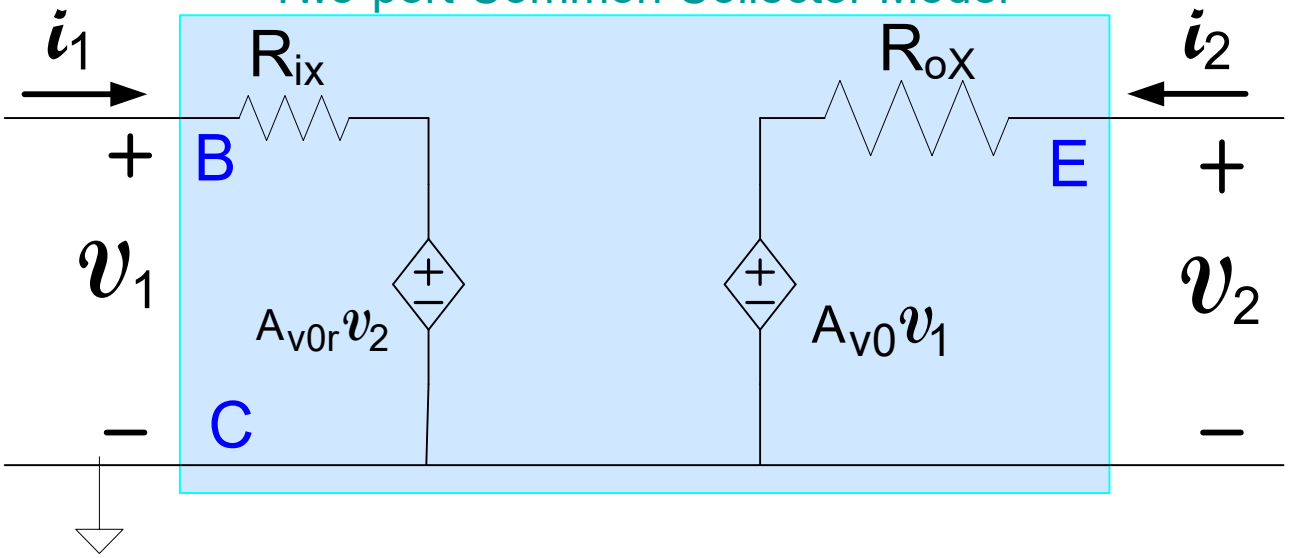
$$R_{0X} = \left(\frac{1}{g_m + g_\pi + g_o}\right) \qquad A_{V0} = \left(\frac{g_m + g_\pi}{g_m + g_\pi + g_o}\right)$$

Two-port model for Common Collector Configuration





Two-port Common Collector Model



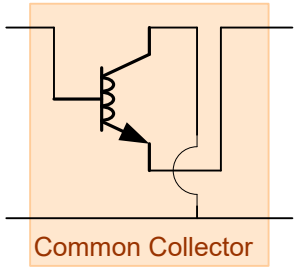
$R_{iX}=r_\pi$

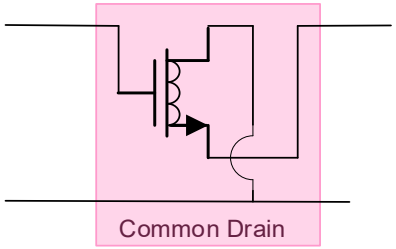
$A_{VOr}=1$

$$R_{0X} = \left(\frac{1}{g_m + g_\pi + g_o} \right) \cong \frac{1}{g_m}$$

$$A_{V0} = \left(\frac{g_m + g_\pi}{g_m + g_\pi + g_o} \right) \cong 1$$

Two-port model for Common Collector Configuration





$A_{VR} = 1$ $A_{VR} = 1$

$R_{in} = r_\pi$ $A_{V0} = 1$ $R_0 = \frac{1}{g_m}$ $R_{in} = \infty$ $A_{V0} = 1$ $R_0 = \frac{1}{g_m}$

In terms of operating point and model parameters:

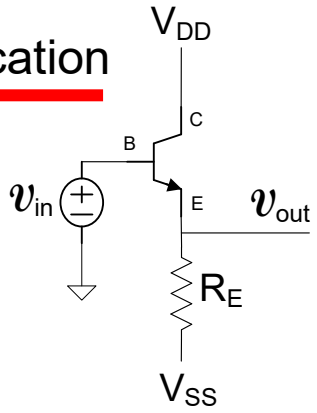
$R_{in} = \frac{\beta V_t}{I_{CQ}}$ $A_{V0} = 1$ $R_0 = \frac{V_t}{I_{CQ}}$ $R_{in} = \infty$ $A_{V0} = 1$ $R_0 = \frac{V_{EB}}{2I_{DQ}}$

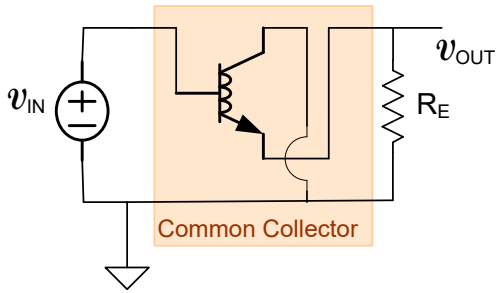
Characteristics:

- Input impedance is mid-range (infinite for MOS)
- Voltage Gain is nearly 1
- Output impedance is very low
- Slightly non-unilateral (critical though in increasing input impedance when R_E added)
- Widely used as a buffer

Common Collector Configuration

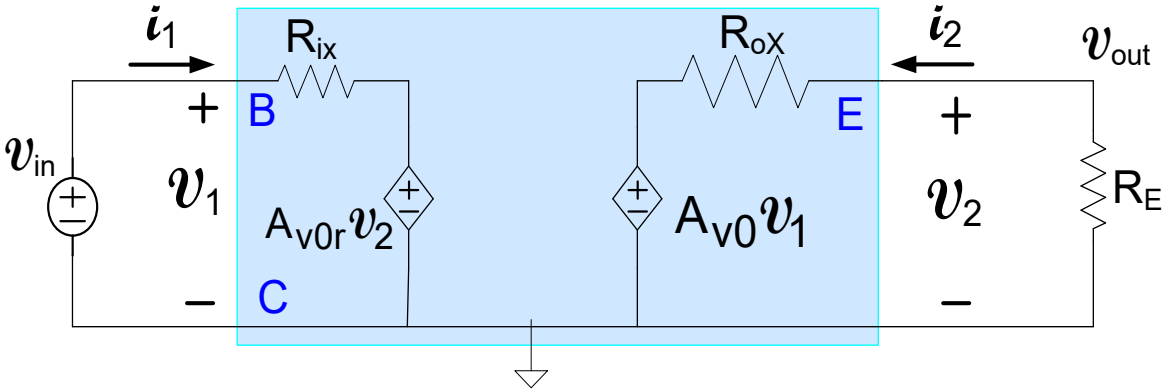
Consider the following popular CC application





Determine R_{in}, R_0, and A_V

(this is not asking for a two-port model for the CC application; R_{in} and A_V defined for no additional load on output, R_o defined for short-circuit input)



$$\frac{g_m}{g_{RE}} = \frac{I_{CQ}R_E}{V_t} >> 1$$

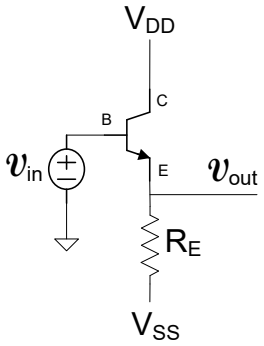
$$A_V = A_{V0}\frac{g_{ox}}{g_{ox}+g_{RE}} = \frac{g_m+g_\pi}{g_m+g_\pi+g_o}\left(\frac{g_m+g_\pi+g_o}{g_m+g_\pi+g_o+g_{RE}}\right) = \frac{g_m+g_\pi}{g_m+g_\pi+g_o+g_{RE}} \cong \frac{g_m}{g_m+g_{RE}} \overset{if\ g_m>>g_{RE}}{\cong} 1$$

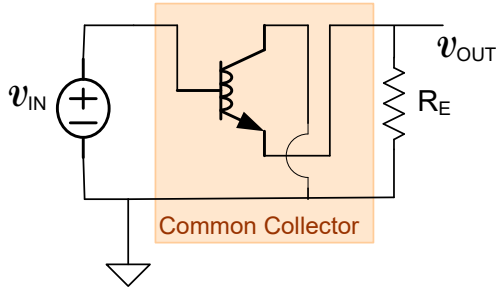
$$v_{in} = i_1 R_{ix} + A_{v0r}A_{v0}\frac{g_{0X}}{g_{0X}+g_{RE}}v_{in} \rightarrow R_{in} = \frac{r_\pi}{1-\frac{g_m+g_\pi}{g_m+g_\pi+g_o+g_{RE}}} = r_\pi\frac{g_m+g_\pi+g_o+g_{RE}}{g_o+g_{RE}} \overset{g_{RE}>>g_o}{\cong} r_\pi+\beta R_E$$

$$R_0 \cong \frac{1}{g_m+g_{RE}+g_0+g_\pi} = \frac{1}{g_m+g_{RE}} = \frac{R_E}{1+g_mR_E} \overset{g_m>>g_{RE}}{\cong} \frac{1}{g_m}$$

Common Collector Configuration

Consider the following popular CC application

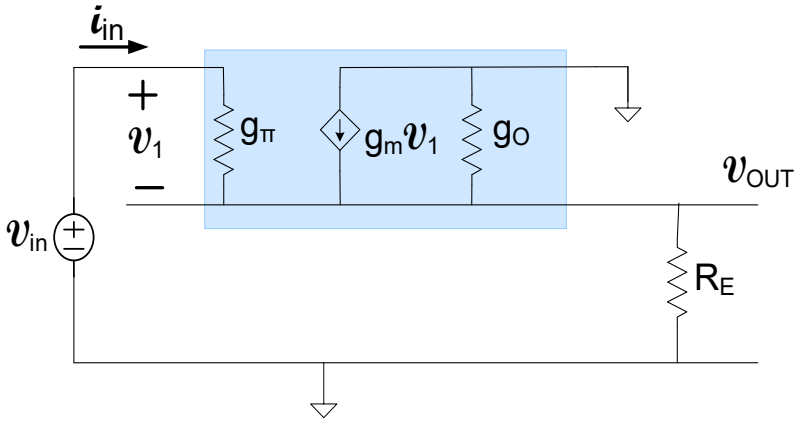




Determine R_{in}, R_0, and A_V

(this is not asking for a two-port model for the CC application ; R_{in} and A_V defined for no additional load on output, R_o defined for short-circuit input)

Alternately, this circuit can also be analyzed directly



$$\frac{g_m}{g_{RE}} = \frac{I_{CQ}R_E}{V_t} >> 1$$

$$v_{out}\left(g_{RE}+g_0+g_\pi\right) = v_{in}g_\pi + g_m v_1$$

$$v_{in} = v_1 + v_{out}$$

$$v_{out}\left(g_m+g_{RE}+g_0+g_\pi\right) = v_{in}\left(g_\pi+g_m\right)$$

$$A_V = \frac{g_\pi+g_m}{g_m+g_{RE}+g_0+g_\pi} \cong \frac{g_m}{g_m+g_{RE}} = \frac{I_{CQ}R_E}{I_{CQ}R_E+V_t} \simeq 1$$

$$i_{in} = g_\pi\left(v_{in}-v_{out}\right)$$

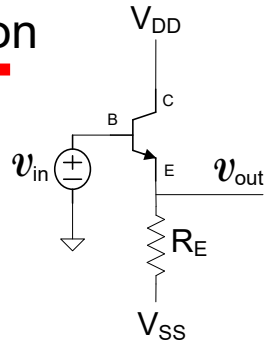
$$v_{out}\left(g_m+g_{RE}+g_0+g_\pi\right) = v_{in}\left(g_\pi+g_m\right)$$

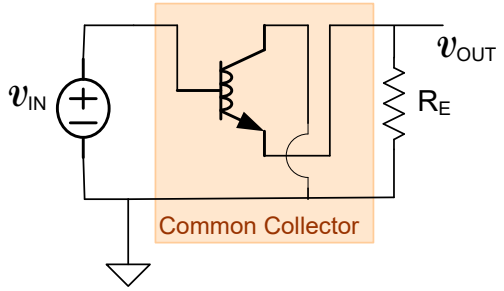
$$i_{in}\left(g_m+g_\pi+g_{RE}+g_0\right) = g_\pi v_{in}\left(g_{RE}+g_0\right)$$

$$R_{in} = r_\pi \frac{g_m+g_\pi+g_o+g_{RE}}{g_o+g_{RE}} \overset{\substack{g_{RE}>>g_o \\ \beta>>1}}{\cong} r_\pi + \beta R_E$$

Common Collector Configuration

Consider the following popular CC application

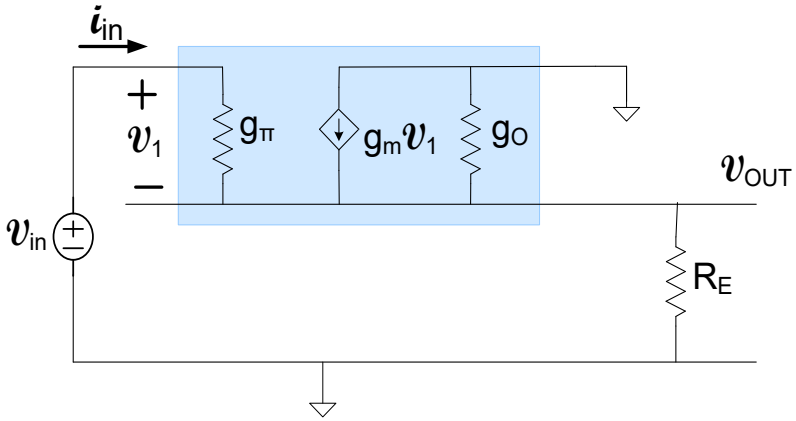


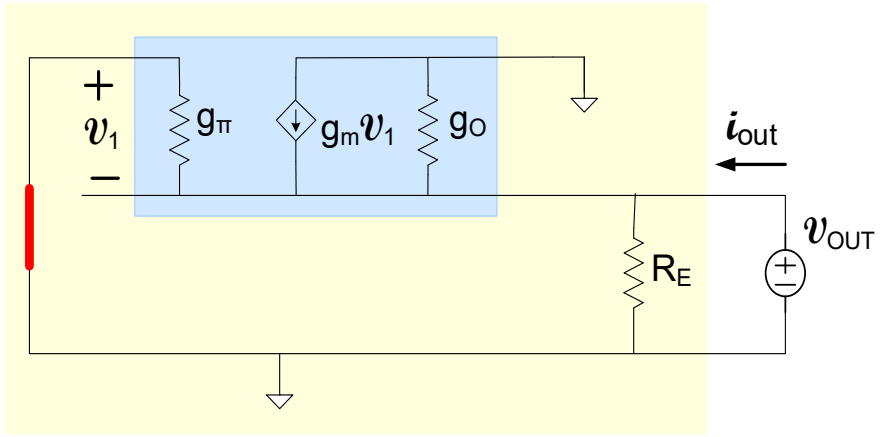


Determine R_{in}, R_0, and A_V

(this is not asking for a two-port model for the CC application; R_{in} and A_V defined for no additional load on output, R_o defined for short-circuit input)

Alternately, this circuit can also be analyzed directly (continued)





To obtain R_0, set $v_{in} = 0$

$$\frac{g_m}{g_{RE}} = \frac{I_{CQ}R_E}{V_t} >> 1$$

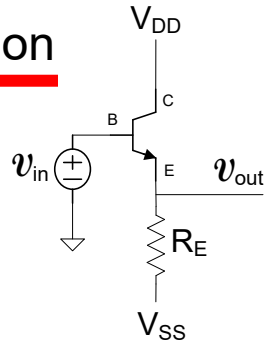
$$i_{out} = v_{out}\left(g_{RE} + g_0 + g_\pi\right) - g_m\left(-v_{out}\right)$$

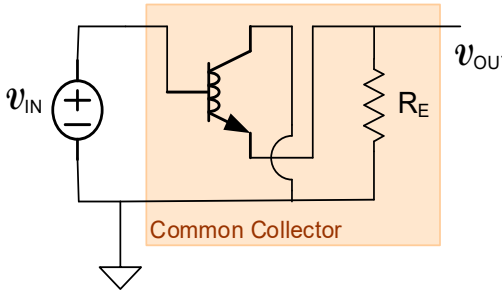
$$R_{out} = \frac{1}{g_m + g_\pi + g_o + g_{RE}} \overset{g_E << g_m}{\cong} \frac{1}{g_m}$$

Common Collector Configuration

Consider the following popular CC application

(this is not asking for a two-port model for the CC application, – R_{in} and A_V defined for no additional load on output, R_o defined for short-circuit input -)





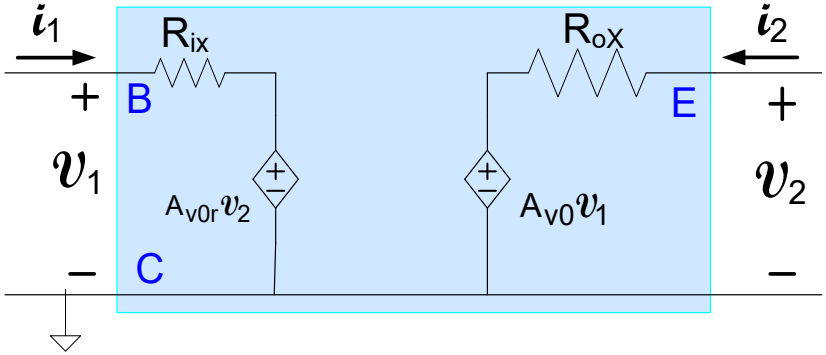
$$A_V = \frac{g_\pi + g_m}{g_m + g_{RE} + g_0 + g_\pi} \cong \frac{g_m}{g_m + g_{RE}} = \frac{I_{CQ}R_E}{I_{CQ}R_E + V_t} \cong 1$$

$$R_{in} = r_\pi \frac{g_m + g_\pi + g_o + g_{RE}}{g_o + g_{RE}} \overset{g_{RE} >> g_o}{\cong} r_\pi + \beta R_E$$

$$R_{out} = \frac{1}{g_m + g_\pi + g_o + g_{RE}} \overset{g_E << g_o}{\cong} \frac{1}{g_m}$$

Question: Why are these not the two-port parameters of this circuit?

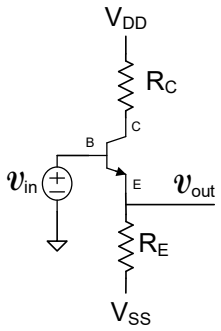
- R_{in} defined for open-circuit on output instead of short-circuit (see previous slide : -2 slides)
- $A_{V0r} \neq 0$

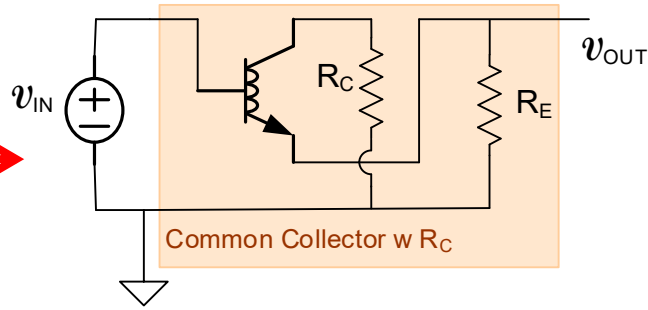


Common Collector Configuration with R_C

Consider the following CC application

(though not real common, sometimes a resistor is included in the collector)





It can be readily shown that unless R_C is very large, it has little effect on the performance and have same expressions for A_V, R_{IN}, and R_{OUT}

$$A_V \cong \frac{g_m}{g_m + g_E} = \frac{I_{CQ}R_E}{I_{CQ}R_E + V_t} \cong 1$$

$$R_{in} \cong r_\pi + \beta R_E$$

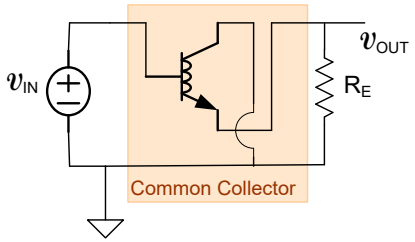
$$R_{out} \cong \frac{1}{g_m}$$

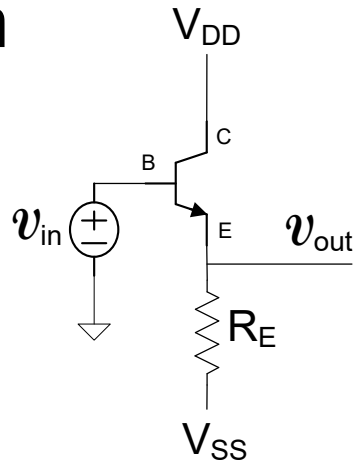
Intuitively this can be expected since if g_0 is neglected, R_C is in series with a current source in the ss BJT model

Common Collector Configuration

For this popular CC application

(this is not a two-port model for this CC application)





Small signal parameter domain

$$A_V = \frac{g_\pi + g_m}{g_m + g_{RE} + g_0 + g_\pi} \overset{if\ g_m >> g_{RE}}{\cong} 1$$

$$R_{in} \overset{g_E >> g_o}{\cong} r_\pi + \beta R_E$$

$$R_0 \cong \frac{R_E}{1+g_m R_E} \overset{g_m R_E >> 1}{\cong} \frac{1}{g_m}$$

Operating point and model parameter domain

$$A_V \cong \frac{I_{CQ}R_E}{I_{CQ}R_E + V_t} \overset{I_{CQ}R_E >> V_t}{\cong} 1$$

$$R_{in} \overset{I_{CQ}R_E >> V_t}{\cong} r_\pi + \beta R_E$$

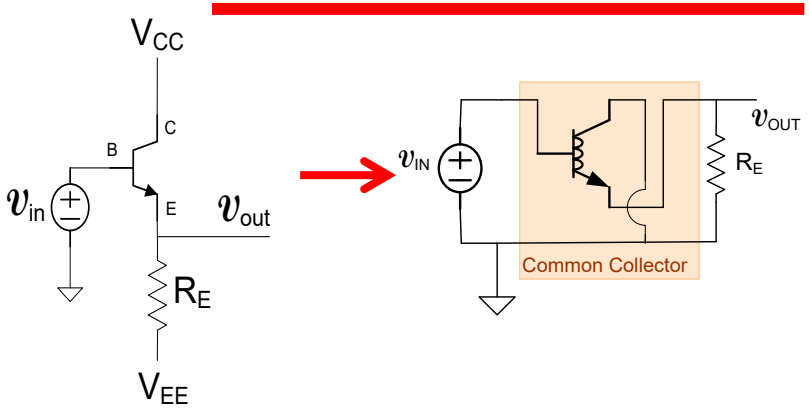
$$R_0 \overset{I_{CQ}R_E >> V_t}{\cong} \frac{V_t}{I_{CQ}}$$

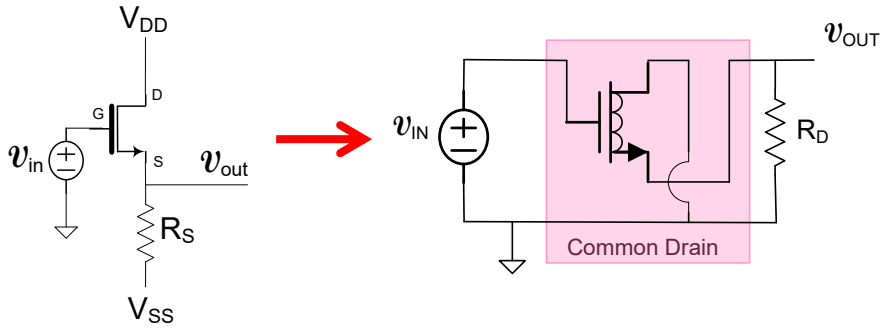
Characteristics:

- Output impedance is low
- A_{V0} is positive and near 1
- Input impedance is very large
- Widely used as a buffer
- Not completely unilateral but output-input transconductance (or A_{Vr}) is small and effects are generally negligible though magnitude same as A_V

Common Collector/Common Drain Configurations

For these popular CC/CD applications (not two-port models for these applications)





$$A_V = \frac{g_\pi + g_m}{g_m + g_E + g_0 + g_\pi} \overset{if\ g_m >> g_E}{\cong} 1$$

$$R_{in} \overset{g_E >> g_o}{\cong} r_\pi + \beta R_E$$

$$R_0 \cong \frac{R_E}{1+g_m R_E} \overset{g_m R_E >> 1}{\cong} \frac{1}{g_m}$$

$$A_V = \frac{g_m}{g_m + g_S + g_0} \overset{if\ g_m >> g_S}{\cong} 1$$

$$R_{in} = \infty$$

$$R_0 \cong \frac{R_S}{1+g_m R_S} \overset{g_m R_S >> 1}{\cong} \frac{1}{g_m}$$

In terms of operating point and model parameters:

$$A_V \cong \frac{I_{CQ} R_E}{I_{CQ} R_E + V_t} \overset{I_{CQ} R_E >> V_t}{\cong} 1 \qquad R_0 \overset{I_{CQ} R_E >> V_t}{\cong} \frac{V_t}{I_{CQ}}$$

$$R_{in} \overset{I_{CQ} R_E >> V_t}{\cong} r_\pi + \beta R_E$$

$$A_V \cong \frac{2 I_{DQ} R_S}{2 I_{DQ} R_S + V_{EBQ}} \overset{if\ 2 I_{DQ} R_S >> V_{EBQ}}{\cong} 1$$

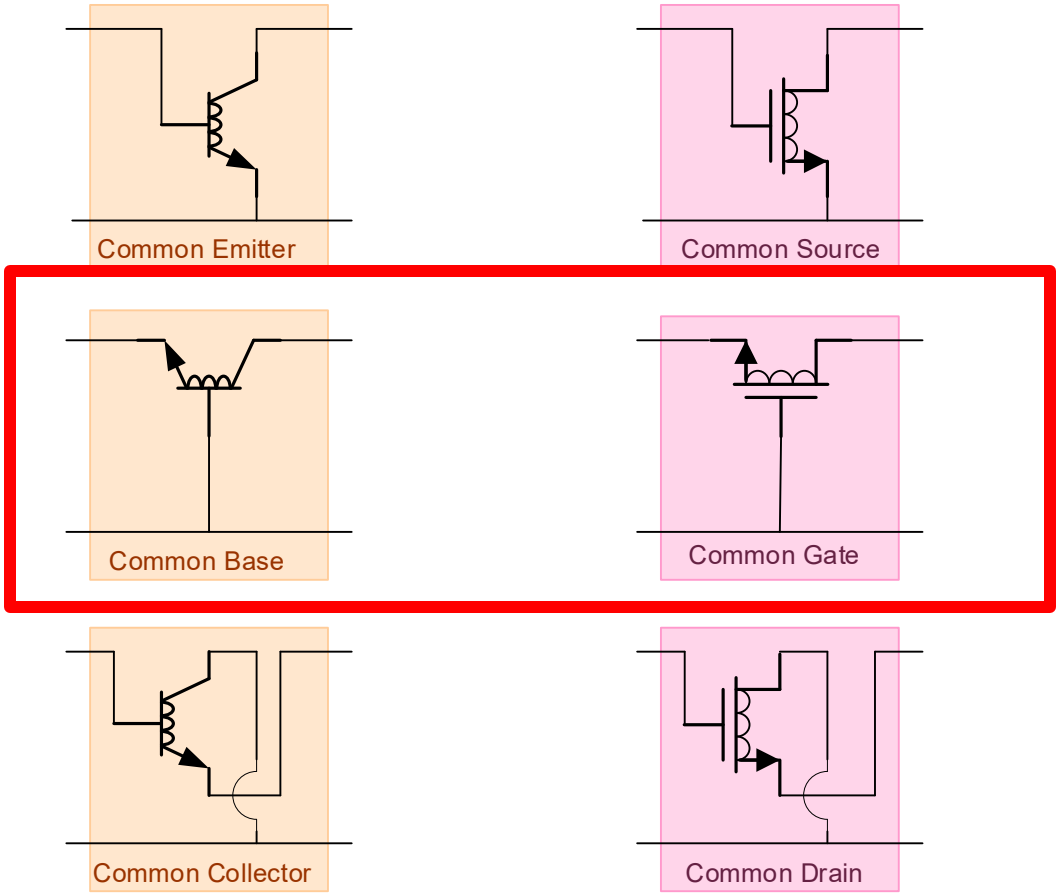
$$R_0 \cong \frac{V_{EBQ} R_S}{V_{EBQ} + 2 I_{DQ} R_S} \overset{2 I_{DQ} R_S >> V_{EBQ}}{\cong} \frac{V_{EBQ}}{2 I_{DQ}}$$

$$R_{in} = \infty$$

- Output impedance is low
- A_{V0} is positive and near 1
- Input impedance is very large
- Widely used as a buffer
- Not completely unilateral but output-input transconductance is small

Consider Common Collector/Common Drain Two-port Models

Remains to study the Common Base/Common Gate configuration



- Will focus on Bipolar Circuit since MOS counterpart is a special case obtained by setting $g_{\pi}=0$
- Will consider both two-port model and a widely used application

Stay Safe and Stay Healthy !

End of Lecture 31